NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

THESIS

SPEED, POWER CONSUMPTION, AND IMPEDANCE IN GALLIUM ARSENIDE IC INTERCONNECTION CIRCUITS

by

Hugh Joseph Huck III

September, 1996

Thesis Advisor: Douglas J. Fouts

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REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE September, 1996	3. REPORT TYPE AND DATES COVERED Master's Thesis

4. TITLE AND SUBTITLE
SPEED, POWER CONSUMPTION, AND IMPEDANCE IN GALLIUM ARSENIDE IC INTERCONNECTION CIRCUITS.

5. FUNDING NUMBERS

6. AUTHOR(S) Huck III, Hugh J.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

The goal of this project is to determine the feasibility of conserving power while maintaining reasonably high speed in Gallium Arsenide integrated circuit interconnection circuits by increasing the characteristic impedance of microstrip or stripline printed circuit board. This thesis presents the modeling and simulation of output driver and input receiver circuits for Gallium Arsenide digital ICs. Impedance controlled printed circuit board transmission lines are also studied. MATLAB is used to model and calculate the impedance that can be obtained using a microstrip and/or stripline printed circuit board interconnect. This information is then used with HSPICE to model and simulate transmission line interconnects. HSPICE is also used to model and simulate the design of the output driver and input receiver circuits for use with the printed circuit board. Finally, the IC is layed out using MAGIC to show differences in circuit size at different impedances.

14. SUBJECT TERMS
Gallium Arsenide, GaAs, Printed Circuit Board, PCB, Speed, Impedance, Power Consumption, Output Drivers, Input Receivers, Interconnect

15. NUMBER OF PAGES 118

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18 298-102

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SPEED, POWER CONSUMPTION, AND IMPEDANCE IN GALLIUM ARSENIDE IC INTERCONNECTION CIRCUITS

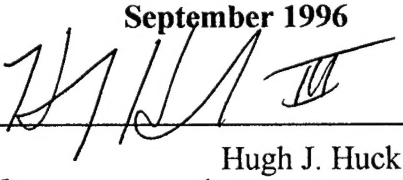
Hugh J. Huck III
Lieutenant, United States Navy
B.S.G.E., United States Naval Academy, 1990

Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
September 1996

Author: 
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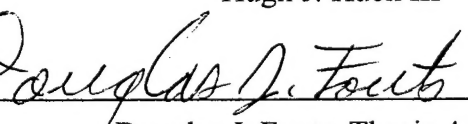
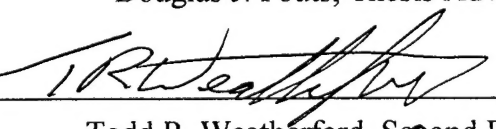
Approved by: 
Douglas J. Fouts, Thesis Advisor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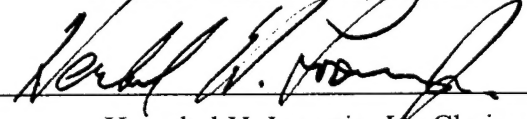
Herschel H. Loomis, Jr., Chairman
Department of Electrical Engineering

ABSTRACT

The goal of this project is to determine the feasibility of conserving power while maintaining reasonably high speed in Gallium Arsenide integrated circuit interconnect circuits by increasing the impedance of microstrip or stripline printed circuit board interconnects. This thesis presents the modeling and simulation of output driver and input receiver circuits for Gallium Arsenide digital ICs. Printed circuit board transmission lines are also studied. MATLAB is used to model and calculate the impedance that can be obtained using microstrip and/or stripline printed circuit board interconnect. This information is then used with HSPICE to model and simulate transmission line interconnects. HSPICE is also used to model and simulate the design of the output driver and input receiver circuits to be used with the previously mentioned output drivers. Finally, the IC is layed out using MAGIC to show the differences in circuit size for drivers with different drive capabilities.

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1. INTRODUCTION

A. ADVANTAGES/DISADVANTAGES OF USING GaAs DIGITAL COMPONENTS IN SYSTEMS

Gallium arsenide (GaAs) integrated circuit technology began in the 1960s. Initially, it was primarily used in the areas of microwaves and optics. Eventually, gallium arsenide logic circuits were developed that were faster than the fastest silicon ECL circuits. Furthermore, silicon ECL circuits require much more power than GaAs circuits.

There are some disadvantages of using GaAs instead of silicon. First of all, the noise margins of gallium arsenide logic are smaller than that of silicon. Gallium arsenide uses metal-on-semiconductor gates. A schottky diode forms at this junction and prevents the gate to source voltage (Vgs) from exceeding 0.7 volts. Leakage currents in GaAs devices are also a problem in many circuits [Ref. 1]. Silicon fabrication technology is more advanced. GaAs is not in as much demand as silicon, thus there are fewer companies producing GaAs ICs and economy of scale is not as great as with silicon ICs.

B. SPEED VERSUS POWER CONSUMPTION IN INTERCONNECTION CIRCUITS

Most high-speed integrated circuits that are attached to and interconnected on printed circuit boards use 50-ohm impedance-matched interconnect. The power consumption at this impedance is high if the termination is matched to the characteristic impedance of the interconnect, a necessary restriction for high-speed I/O circuits. Ohm's

law dictates that V / R = I. For ECL logic swings of -1.8 to -0.8 V, the maximum I/O current peak is 0.024 amperes per interconnect. The power per output pin of a GaAs chip can be calculated using the equation P=IV, where I=0.024 amperes, and V=2.0 Volts. The power per output pin becomes 0.048 Watts. A 128 output-pin IC would then consume an average 6.144 Watts just for the output drivers. Using the same equation for greater values of interconnect characteristic impedance and terminating load, we can see that the power consumption is greatly reduced. If the impedance of the interconnect and termination was changed from 50 ohms to 100 ohms, the average current (V/R=I) would change from 0.024 amperes to 0.012 amperes and the average power (P=IV) per output pin would be 0.024 watts. The average power for a 128 output pin IC would change from 6.144 Watts to 3.072 Watts, a 50 percent decrease in power. A substantial decrease in power consumption will result in longer battery life for portable/mobile applications and less heat dissipation.

C. GOALS OF THESIS

The intent of this thesis is to discern if the impedance of the interconnects for GaAs I/O circuitry can be increased while still maintaining a reasonable amount of speed. Power consumption will also be looked at to observe the decrease as the impedance is increased. The first portion of the thesis is devoted to the development of high-impedance printed circuit board (PCB) interconnects and determination of how much the impedance can be increased with current PCB implementation technology.

With this information, calculations are performed to design transmission-line interconnect at different impedances. High-impedance drivers are developed, modeled, and simulated in HSPICE. HSPICE is a registered trademark of Meta-Software and is a simulation program designed to model and simulate electronic circuits, and can model transistor level interconnects [Ref. 4]. Receivers are developed using HSPICE as well. Drivers and receivers are then connected together and used to determine the highest attainable speed at different interconnect impedances. A power consumption analysis is then done to show the decrease in power consumption as the impedance is increased. The final consideration is the layout of the drivers and receivers, and how higher impedances decrease the size of their respective layouts using MAGIC. MAGIC is a registered trademark of the University of California, Berkeley and is a program used to model and lay out transistors on a Gallium Arsenide or Silicon chip [Ref. 9]. Conclusions and recommendations are made in the last chapter.

II. PRINTED CIRCUIT BOARD DESIGN

A. MICROSTRIP DESIGN

In microstrip interconnect design, a dielectric separates a large metal ground plane from small metal strips that are used to carry the signals. Figure 2-1 shows the layout of the microstrip. This arrangement brings into play several factors that can affect high-speed signals. As signal frequency increases, parasitic capacitance, inductance, and transmission-line effects become more pronounced. The thickness and width of the interconnect metal, as well as the dielectric thickness and type, can be manipulated, within limits, to increase or decrease the impedance of the transmission line. Microstrip is popular due to is ease of fabrication and lower cost. A potential problem with the microstrip technique is the limitations in routing that may occur with more complicated boards. [Ref. 3, pg. 5-32]

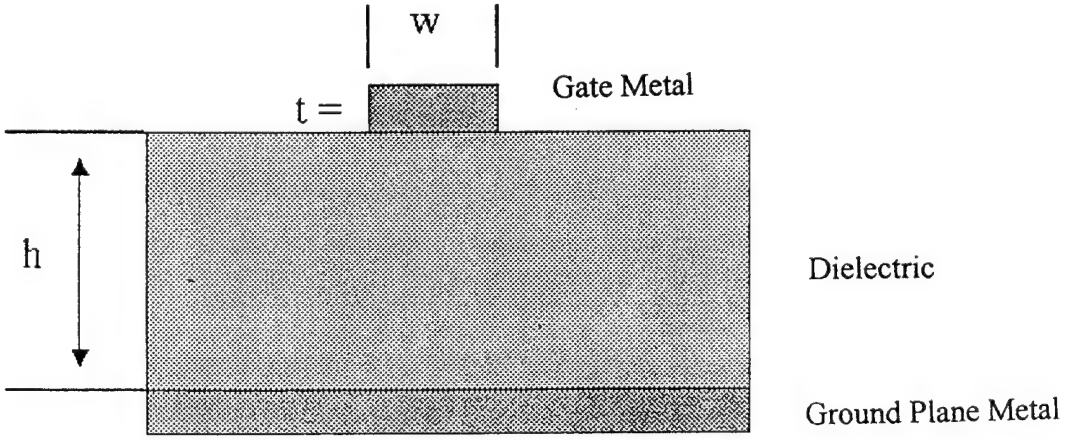

Figure 2-1 Microstrip Design

B. STRIPLINE DESIGN

In stripline design, the interconnect metal is not on the surface of the dielectric. It is placed within the dielectric and between two ground planes. Figure 2-2 shows the layout of the stripline design. Stripline also gives some leeway to design, especially with multiple layer boards, and is used often when high wiring density is a high priority [Ref. 3, pg 5-32] . Other interconnect structures exist for printed-circuit-board interconnect (embedded microstrip, dual asymmetric stripline, coplanar stripline), but were not considered in this thesis because they are not often used in digital system printed circuit boards.

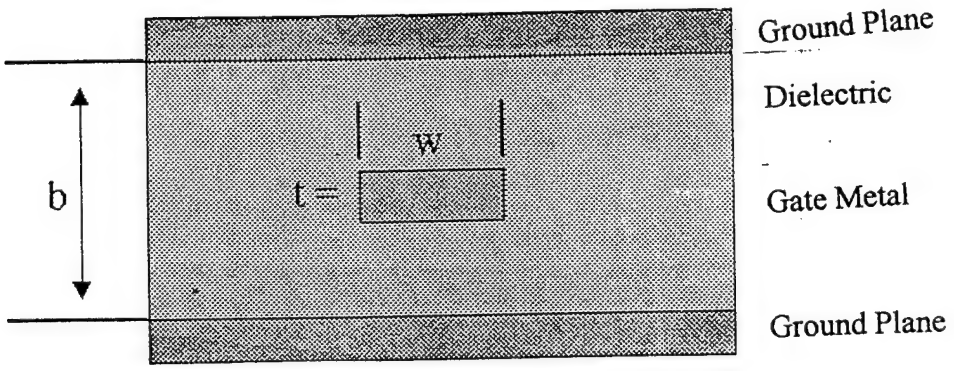

Figure 2-2 Stripline Design

C. CALCULATIONS FOR MICROSTRIP / STRIPLINE IMPEDANCE

1. MATLAB Modeling of Microstrip/Stripline Interconnect

The most important thing to calculate was the range of impedances that can be

attained using the microstrip or stripline approach. These calculations are done in MATLAB. MATLAB is a registered trademark of Meta-Software and is a program used to model and graph mathematical equations [Ref. 8]. Parameter values were needed for these calculations as well as reasonable ranges that could be attained for practical implementations. Dimensions from a local printed circuit board company were used to determine the range that can be attained using current technology. Figure 2-3 shows the current values used in the calculations for the microstrip/stripline impedance design.

VARIABLE	MINIMUM VALUE	MAXIMUM VALUE
Distance from surface layer to buried layer	2.5 millimeters	125 + millimeters
Dielectric constant	4.6	4.6
Trace edge width	5 millimeters	none
Trace edge thickness	0.0007 inches with 0.5 oz. Copper	0.0014 inches with 1 oz. Copper
Distance between etches	5 millimeters	none

Figure 2-3 Range of Values Used in PCB Calculations

With this information, a model can be used to calculate the impedance that could be attained and fabricated. The characteristic impedance equation for microstrip design is [Ref 3, pg 5-32]

$$Z_0 = \frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left(\frac{4h}{0.67\,(0.8w + t)}\right)$$

with
h = dielectric thickness
w = trace width
t = trace thickness
ε_r = dielectric constant relative to air

The equation for stripline calculations is slightly different from microstrip calculations because they are completely embedded, with a ground plane on both sides. The characteristic impedance equation for stripline is

[Ref 3, pg 5-33]

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4b}{0.67\ \pi\ (0.8w + t)}\right)$$

where
b = distance between ground planes
w = trace width
t = trace thickness
$w/(b-t) < 0.35$ and $t/b < 0.25$.

These equations were coded into a MATLAB program in order to get a graphical representation over a range of parameter values to determine just how large a printed circuit board interconnect impedance could be reasonably attained [Appendix A]. Figure 2-4 through Figure 2-9 show the results of the calculations. In Figure 2-4, and Figure 2-5, the trace thickness is set at 0.00035 inches and the dielectric thickness is increased. The characteristic impedance is then plotted at different strip widths. In Figure 2-6 and Figure 2-7, the trace thickness is increased to 0.0007 inches and then plotted again with the previous parameters. In the last two Figures, 2-8 and 2-9, the

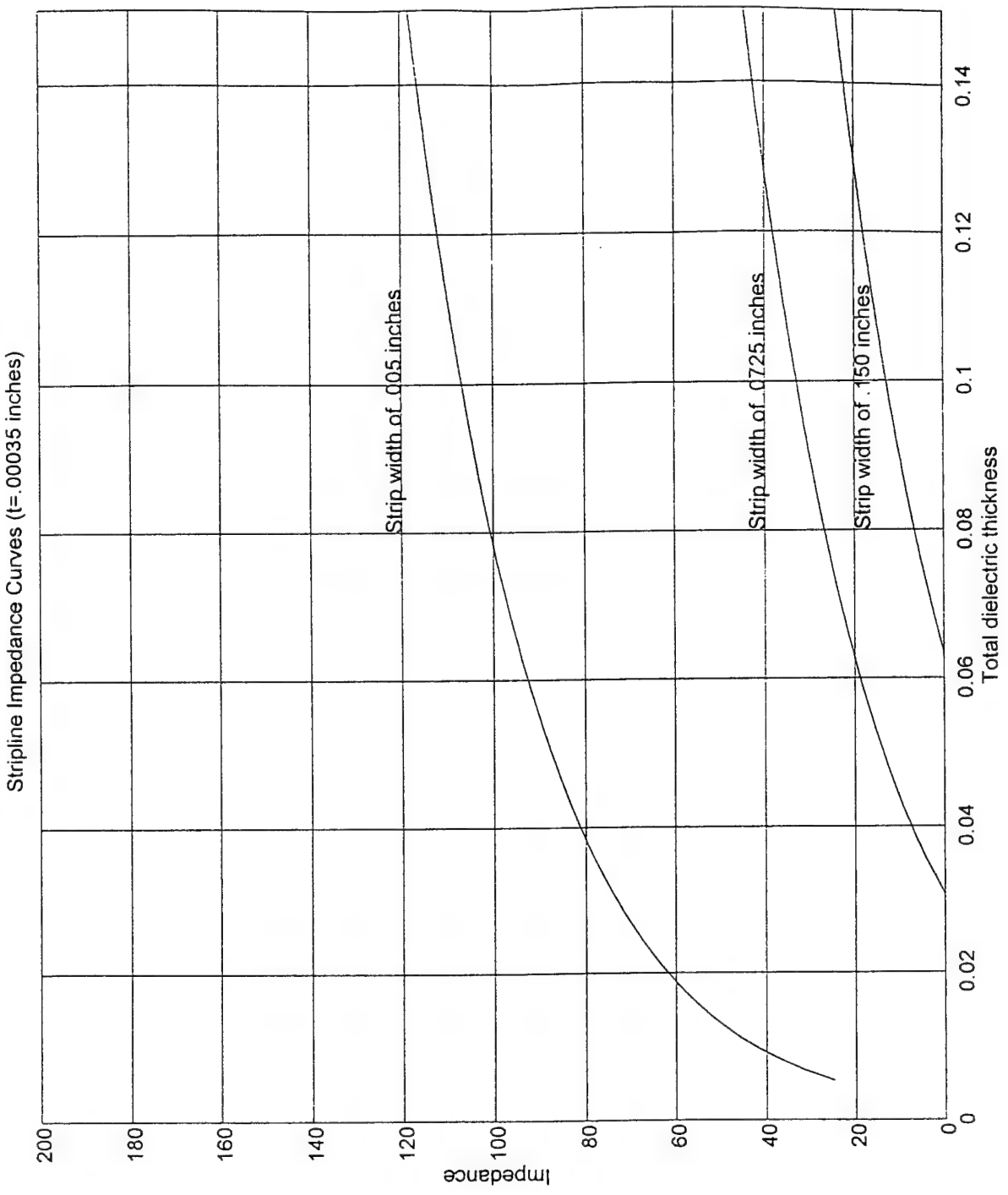

Figure 2-4 Stripline Impedance With t = 0.00035 Inches

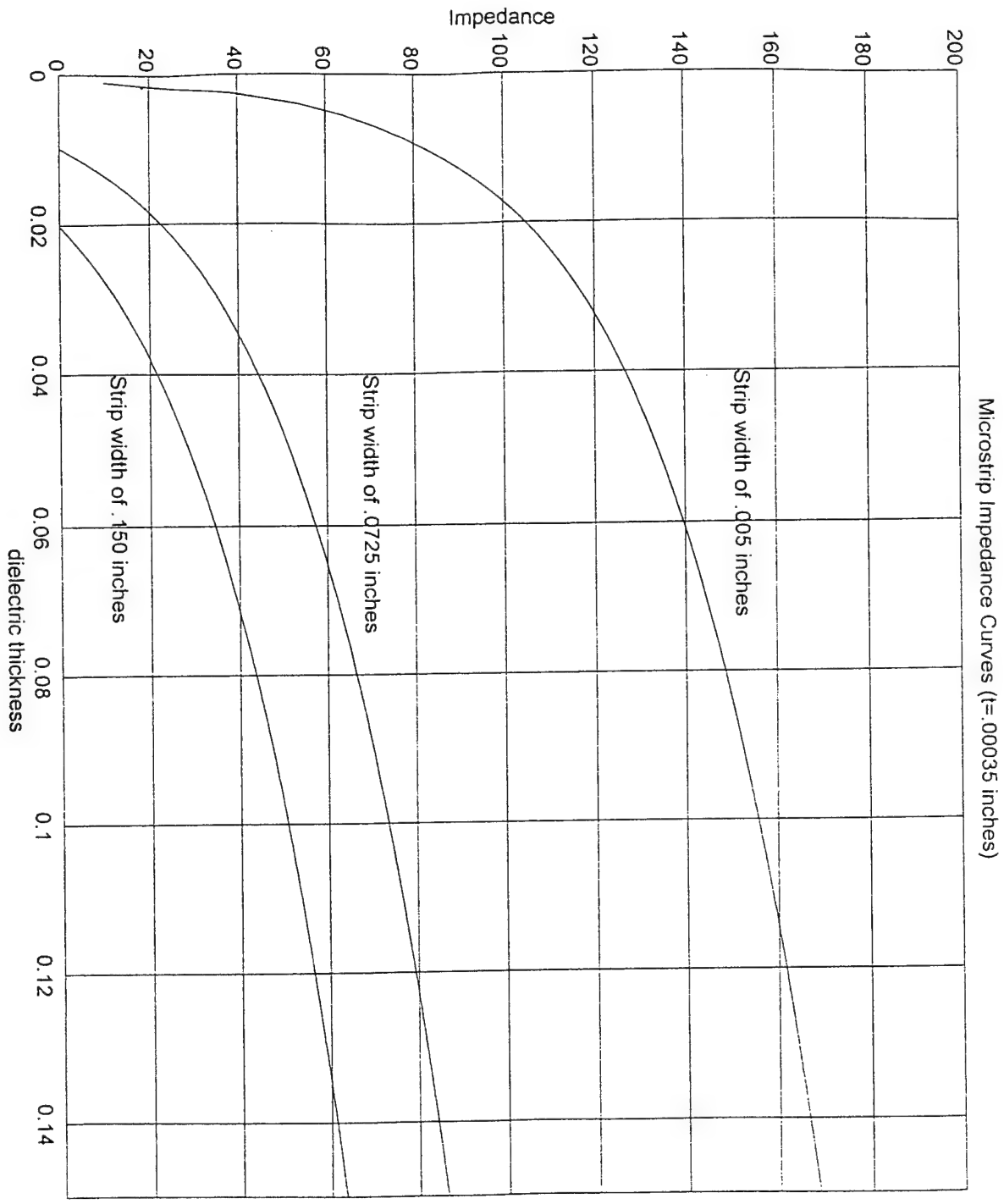

Figure 2-5 Microstrip Impedance With t= 0.00035 Inches

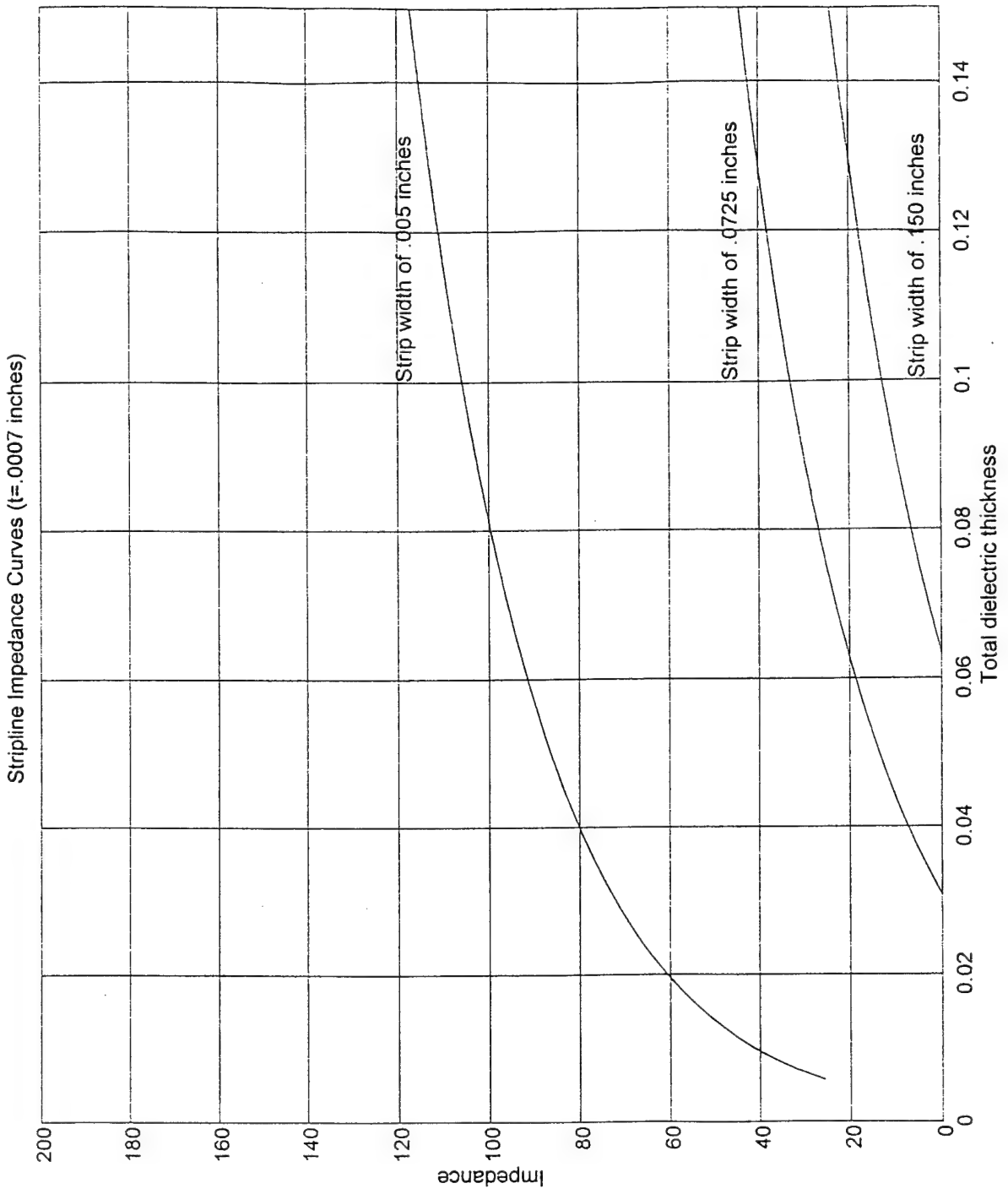

Figure 2-6 Stripline Impedance With t = 0.0007 Inches

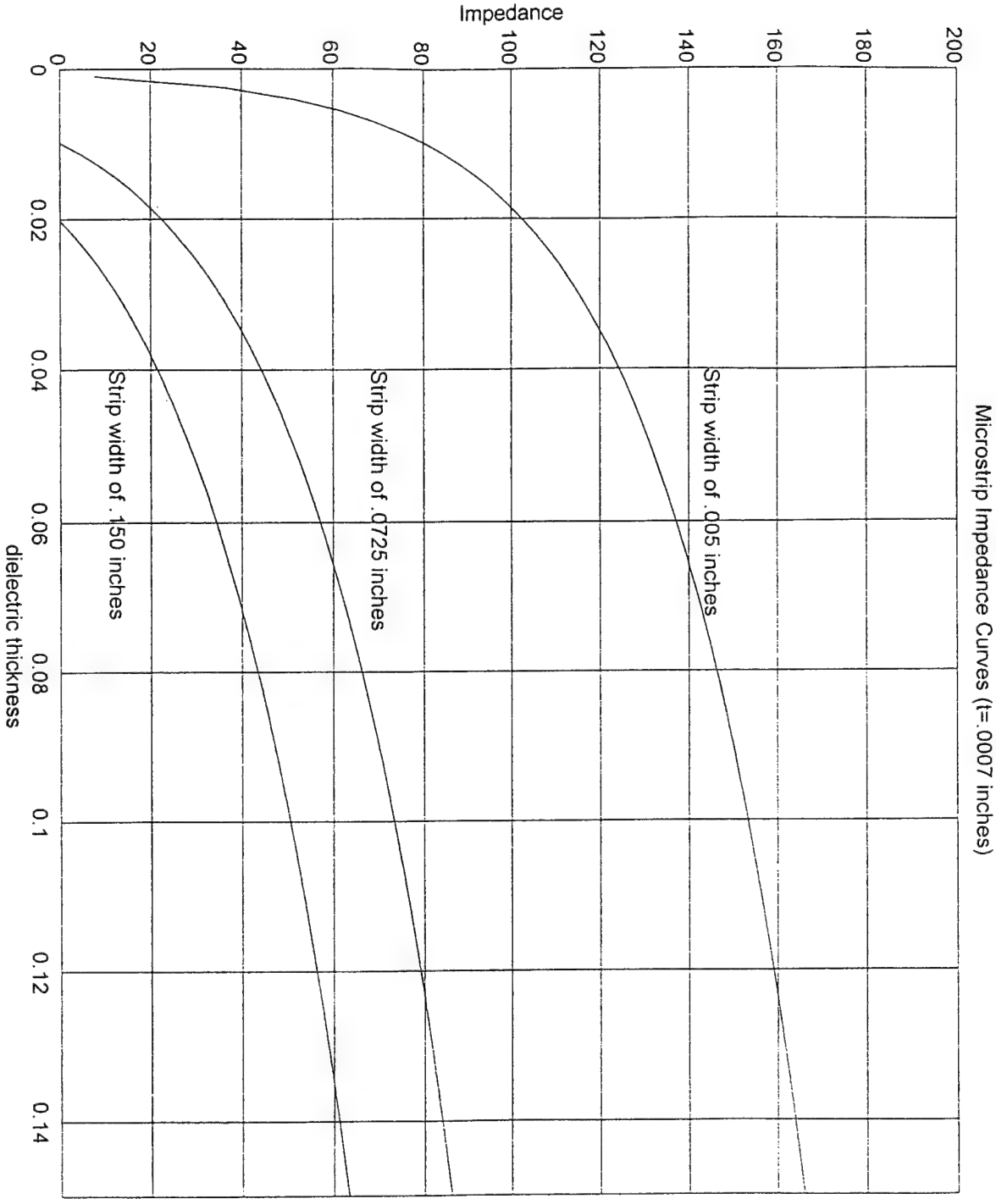

Figure 2-7 Microstrip Impedance With t= 0.0007 Inches

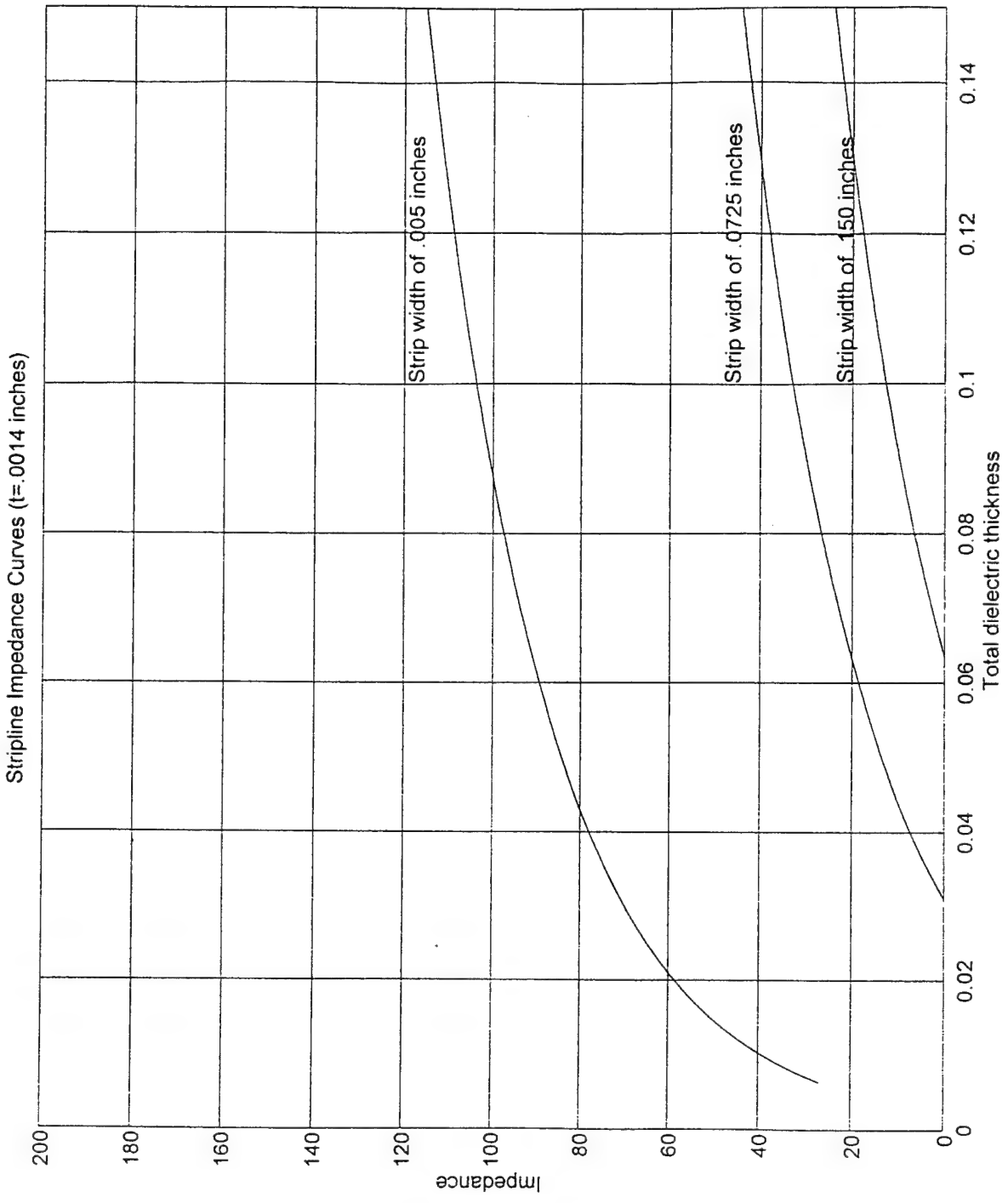

Figure 2-8 Stripline Impedance With t=0.0014 Inches

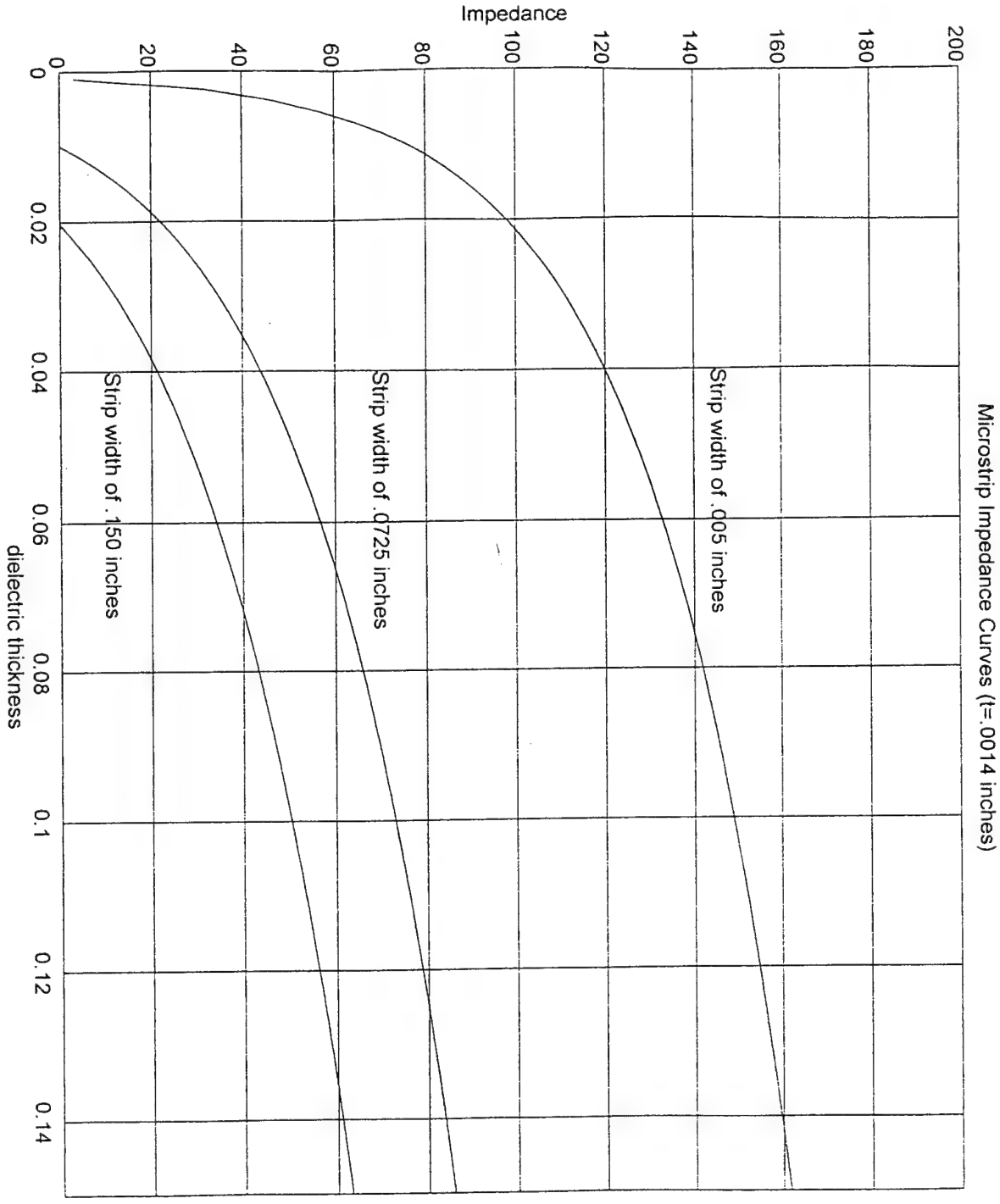

Figure 2-9 Microstrip Impedance Curves With t=0.0014 Inches

the trace thickness is again increased to 0.0014 inches. From these graphs, it was found that the impedance could easily range from 50 to 150 ohms using a strip width of 0.005 inches and a trace width of 0.00035 inches for both microstrip and stripline interconnect. This information proved that typical printed-circuit-board designs could provide three different impedance ranges on the same board and could reasonably be fabricated by a printed-circuit-board fabrication plant.

2. Parasitic Capacitance/Inductance

Once it was determined that the impedance of the interconnect could be 50, 100, or 150 ohms, the next step was to create a model of the PCB interconnect that included all of the possible parasitic capacitances and inductances related to the interconnect. These calculations are important in order to create a transmission-line model of the PCB. The factors that were considered were on-chip bond pad capacitance, bondwire inductance, package capacitance, and board capacitance. Figure 2-10 shows a schematic diagram of the resulting interconnect circuit.

The bond pad parasitic capacitance (CBP) is the on-chip capacitance between the ground plane (back side of the die) and the wire-bond pad. Bond pads are usually 100 by 100 microns, for an area of 10,000 μm^2. Capacitance was then calculated by multiplying 10,000 by 0.06 femto farads/microns^2 to get 600 femto farads. Another capacitance consideration with the bond pad is the fringe capacitance. Since the bond pad is large, the fringe capacitance could be larger. The side of the bond pad (100 microns) was

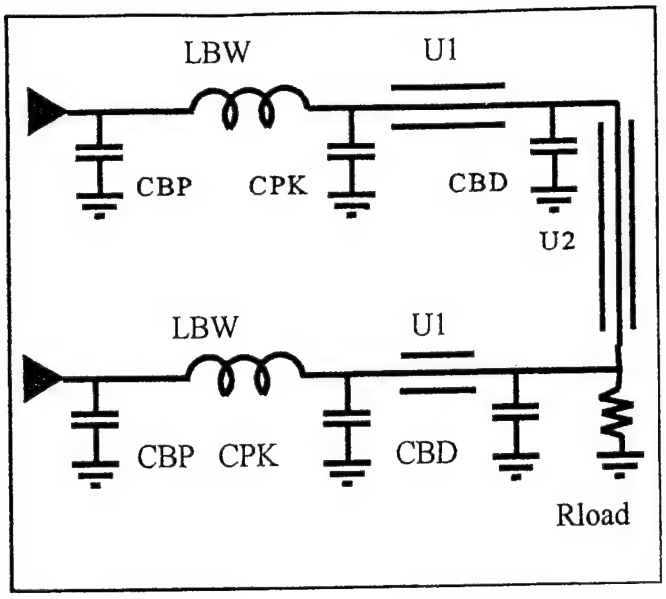

Figure 2-10 Schematic Diagram of Interconnect Circuit

multiplied by 4 and then multiplied by 0.05 femto farads / micron to obtain 20 femto farads. The total bond pad capacitance was the sum of the two totals, 620 femto farads.

Bond wire inductance (LBW) is calculated by figuring the distance of the bondwire from the pad to the chip and assuming that is half of a one- turn inductive loop. The inductance calculation for a single wire loop of this type is

$$L = \frac{\mu}{2\pi} \ln\left(\frac{4h}{d}\right)$$

where
$\mu = 1.257 \times 10^{-8}$ Henrys/Centimeter
h = length of wire
d = diameter of wire

Using an actual packaged GaAs IC, the bond wire was found to be 1/32 inches long and approximately 1/280 inches in diameter. The bond-wire inductance was then calculated to be 7.104 nanoHenrys.

The board capacitance (CBD) was calculated using a width of 0.02 inches and a length of 0.2 inches. A dielectric constant of 4.6 was used for the dielectric, a common value for polyimide or teflon boards used for high speed systems. The board capacitance was calculated to be 206.8 nanoFarads. This represents the parasitic capacitance that exists at the point where the package lead attaches to the PCB.

3. HSPICE Transmission Line Modeling of Printed Circuit Board Interconnect.

Once all the parameters were calculated, the next consideration was to determine if the PCB interconnect could support high-frequency operation at the selected impedances. Using the U transmission model in HSPICE, a 50-ohm transmission line model was created. The U model was decided upon because it is the lossy transmission line model, which is used when the effects of loss are significant. The U model (or element) allows for frequency-dependent characteristic impedance, dispersion, and attenuation [Ref. 4, page 2-36]. The transmission-line HSPICE program is located in Appendix B.

The results of the HSPICE DC plot are shown in Figure 2-11. In this plot, the intention was to find the acceptable voltage swing at the load resistor. The DC model ignored the capacitive and inductive effects and was used for checking circuit

connectivity. The HSPICE AC model is shown in Figures 2-12 through 2-14. In these models, everything was taken into account and was used to determine the highest frequency signal the PCB interconnect could propagate, as well as how the output waveform would look. As shown, the output could reach a period of close to 1.5 nanoseconds. The output waveforms were found to be satisfactory to this point. The difference between the waveforms for 50-, 100-, and 150-ohm interconnect seemed to be small to negligible at the output. This was surprising, considering that the assumption was that the parasitic capacitance in conjunction with the higher resistance would drastically affect the RC time constant of the PCB interconnect.

In this chapter, the maximum allowable impedance of the printed circuit board is calculated and found to be 150 Ohms. The interconnect between the chip and the printed circuit board, needs to be designed and simulated. In the next chapter, drivers for 50-, 100-, and 150-ohms are designed and simulated to ensure that proper voltages and reasonably high speeds across the interconnect are maintained.

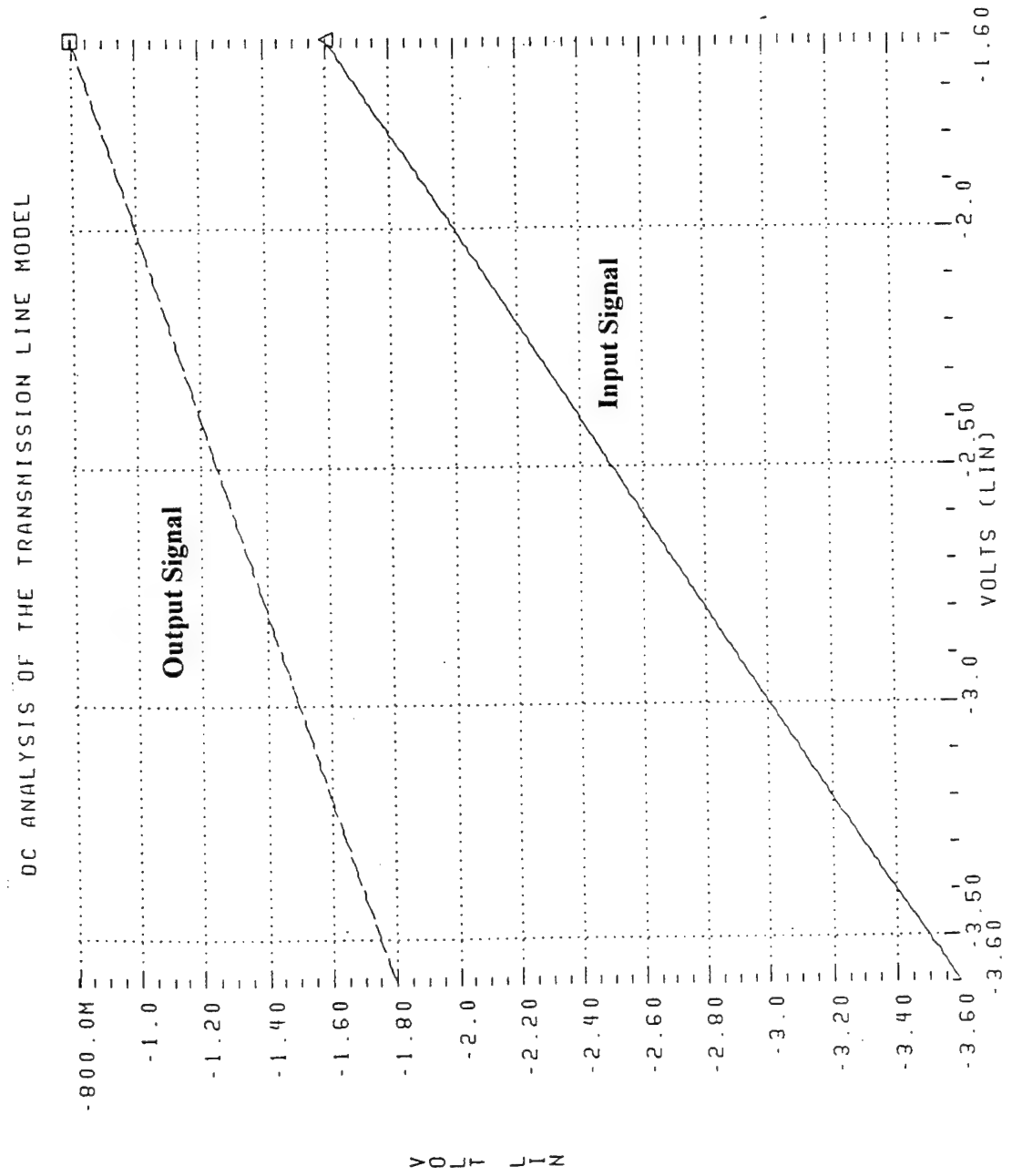

Figure 2-11 DC Analysis of PCB Transmission Line Model

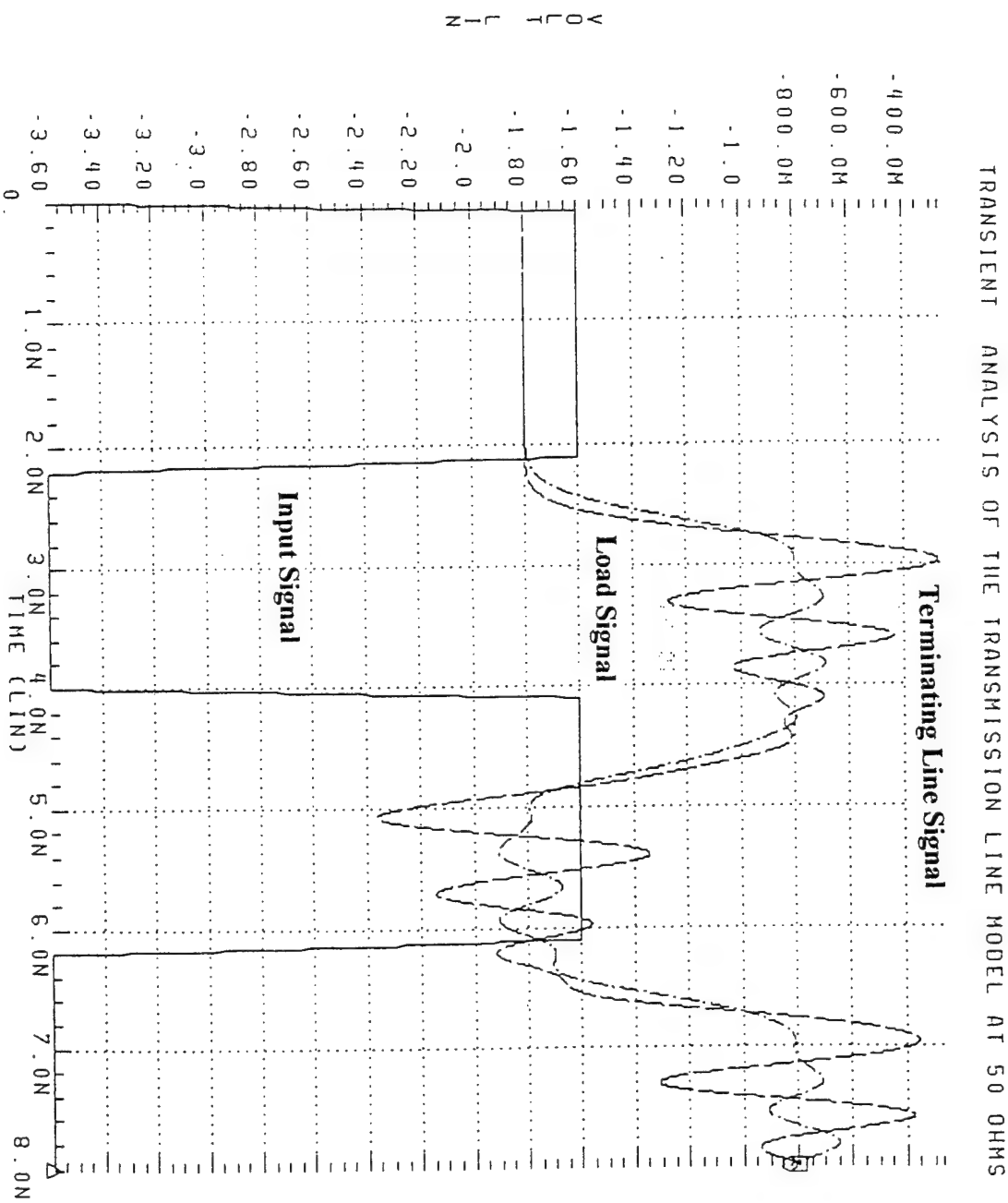

Figure 2-12 Transient Analysis of PCB Transmission Line at 50 Ohms

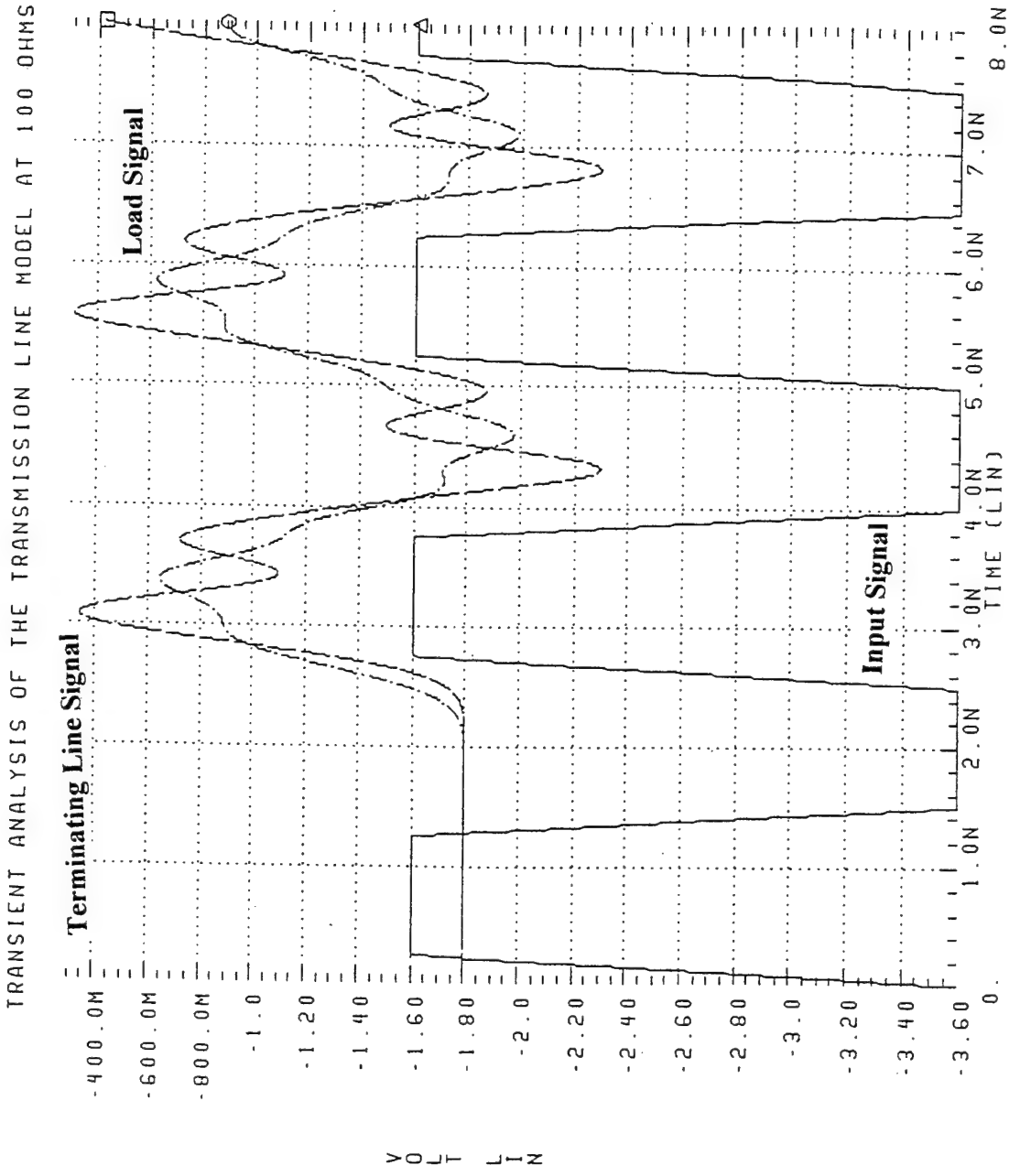

Figure 2-13 Transient Analysis of PCB Transmission Line at 100 Ohms

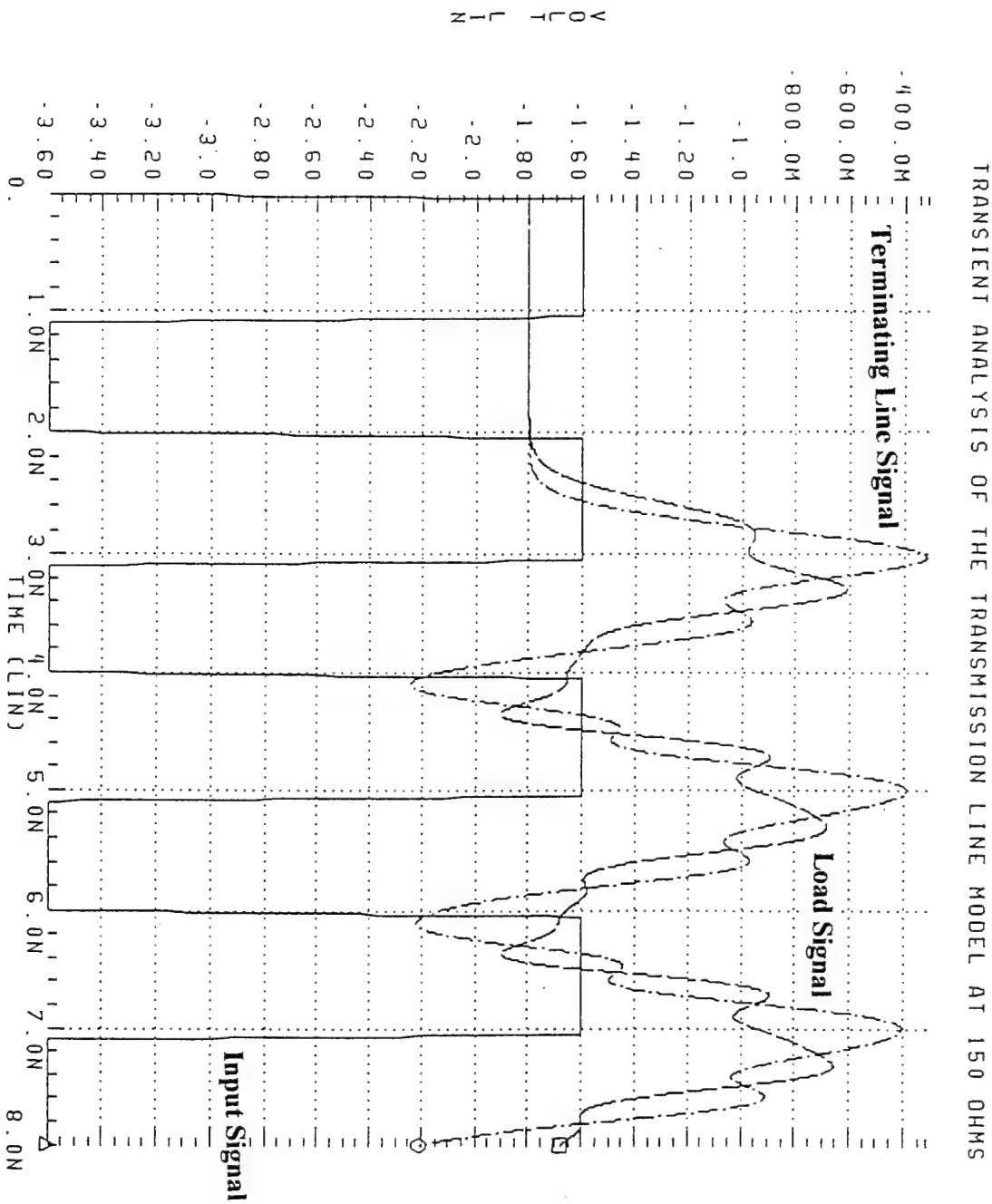

Figure 2-14 Transient Analysis of PCB Transmission Line at 150 Ohms

III. GALLIUM ARSENIDE DRIVER DESIGN

A. DRIVER CHARACTERISTICS

A driver is the output interface circuit between the main part of the GaAs chip and the printed circuit board (PCB). It is used to convert from the smaller on-chip voltage swings to the larger off-chip voltage swings. For this thesis, GaAs digital circuits are assumed to be operated from a -2.0 volt power supply. The driver required for this circuit must convert the on-chip voltage swing of -1.35 volts to -1.95 volts to an off-chip voltage swing of -0.8 volts to -1.8 volts. Figure 3-1 shows a typical GaAs digital IC block diagram, including both drivers and receivers.

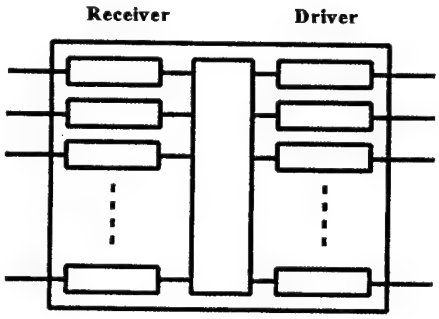

Figure 3-1 Typical GaAs Digital IC Block Diagram

Certain considerations were used to decide on what type of circuit was to be used in designing the output driver. The most important thing was to attain -1.8 volts on the output for an output low. A basic source follower was decided upon because of the low output impedance.

The circuit known as a super buffer was selected to be the input amplifier for the output driver circuit due to its gain and ability to drive a moderately high load capacitance. The superbuffer is a quasi-complementary output driver in which an inverter is paired with a source-follower driver. This setup aids in increasing the noise margins by using two different transistor pairs. The only setback to using superbuffers is that this circuit does cause a momentary current spike on the VDD and ground rails when transitioning from high to low. Ample power and ground buses are required to prevent dynamic upset of the other logic elements. [Ref. 1, page 214-215]

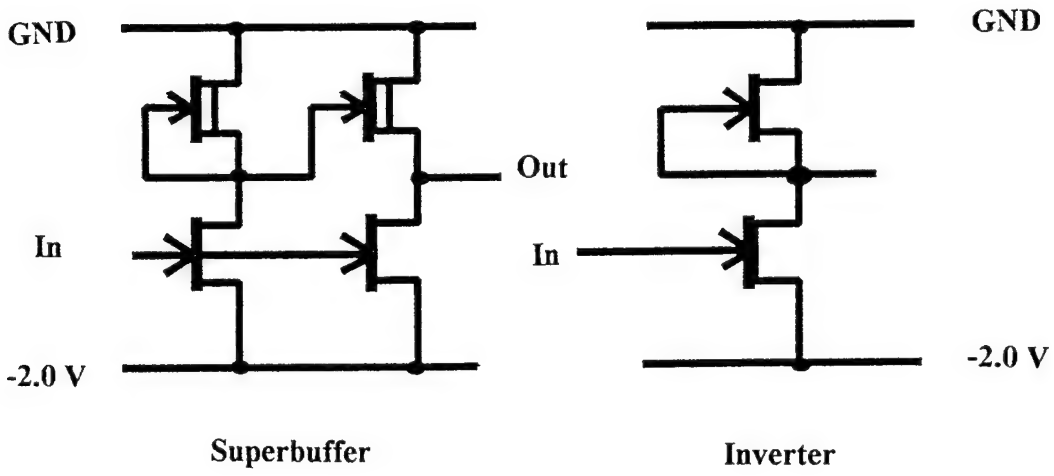

Figure 3-2 Superbuffer / Inverter Design

Diodes were used to help maintain the low output at -1.8 volts when the EFET source follower was shut off. The diodes do not greatly affect the circuit voltage when the EFET is turned on and producing -0.8 volts. An enhancement field effect transistor was used for the source follower because of its ability to "completely" shut off when the

output is at -1.6 volts.

B. HSPICE MODELING OF DRIVER CIRCUIT

1. Standalone Modeling

The circuit topology shown in Figure 3-3 was used for driver simulations in HSPICE. The superbuffer was created first, with the goal to create the required voltage swing needed to turn on and off the EFET used as a source follower. The inverter portion of the superbuffer was created with a gate width to length ratio of 16:1. This was

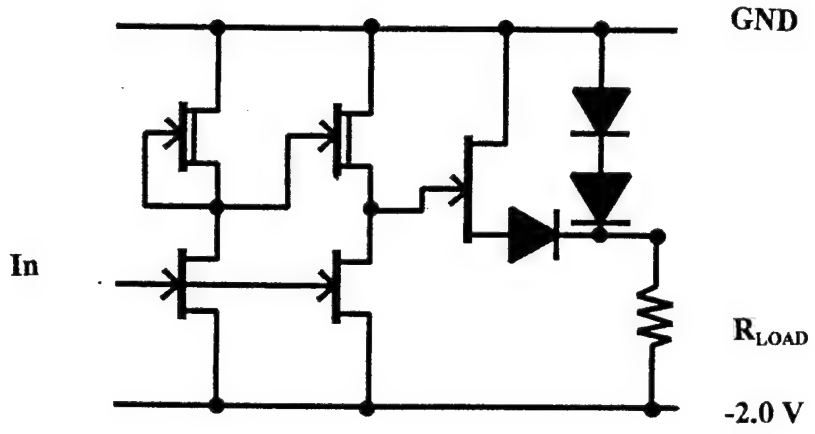

Figure 3-3 Driver Circuit

done to keep the input at a high impedance, as well as to maintain a reasonable noise margin. After the superbuffer was designed with the proper voltage swing, the EFET was added to the output of the superbuffer. At first, the DFET and EFET were both tested to

see if the speed of the EFET was significantly slower than that of the DFET. The speed difference was found to be less than significant and it was easier to attain the desired output voltages with the EFET. The EFET was expected to have a large channel width to accommodate the required voltage swing. The size of the EFET was found to be much larger than expected to obtain the required voltage swing, as well as for attaining the desired output high voltage of -1.8 volts. As the EFET was widened, the circuit gain became closer to 1. The drawback found with widening the gate was that the gate capacitance increases as well, which became a factor as frequency is increased. A 0.8 by 500 micron gate was the smallest EFET that met the required output voltage specifications with a 50-ohm load.

When the load impedance was increased to 100 ohms, the driver using an EFET with a 0.8 by 500 micron gate was out of specifications, with the output high voltage being too high and the capacitance being a bigger factor in the speed of the circuit. The gate was found to be optimized at a size of 0.8 by 200 microns, which yielded a sufficient output high voltage and less capacitance. The trend continued at 150 ohms. The gate was optimized to 0.8 by 120 ohms. Appendix B contains the HSPICE code used in designing the drivers and testing their DC characteristics. Figures 3-4 through 3-6 show the DC characteristics of the input versus the output voltage for the 50-, 100-, and 150-0hm drivers. A significant observation was made while creating these drivers. As the impedance was increased, the size of the source follower EFET decreased, which increased the maximum frequency by decreasing the gate capacitance of the source

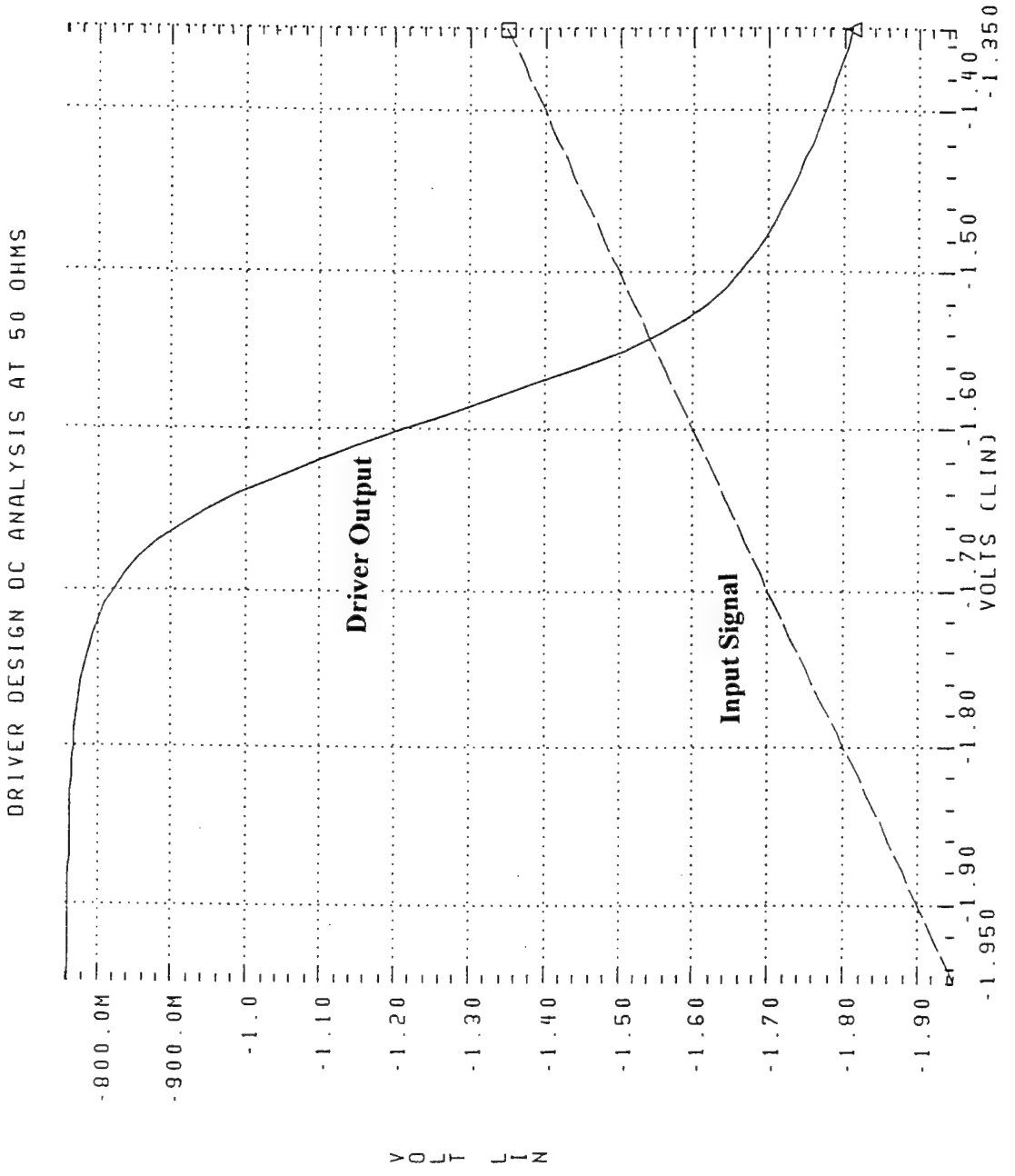

Figure 3-4 DC Analysis of Driver Design for 50-Ohm Load

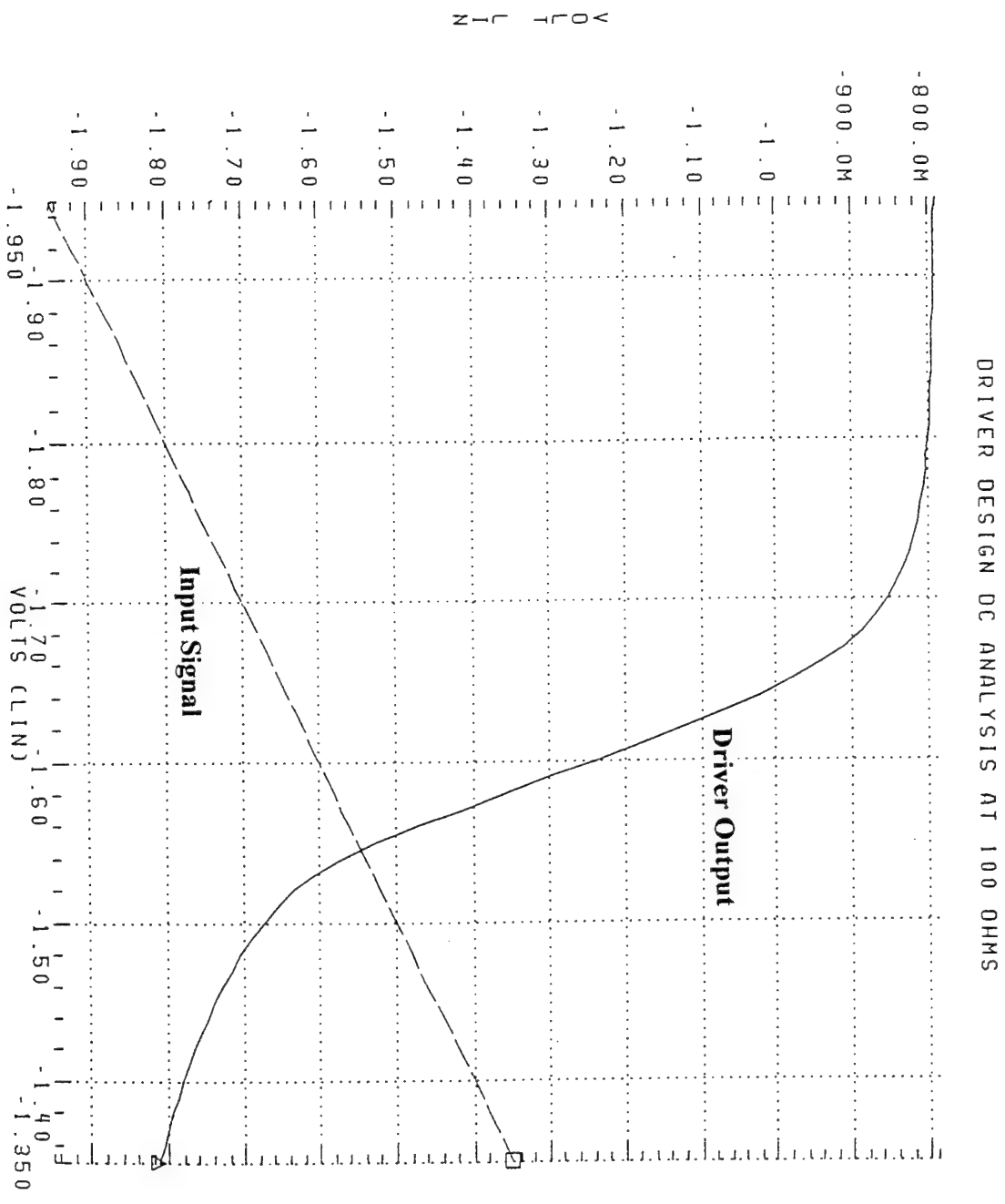

Figure 3-5 DC Analysis of Driver Design for 100-Ohm Load

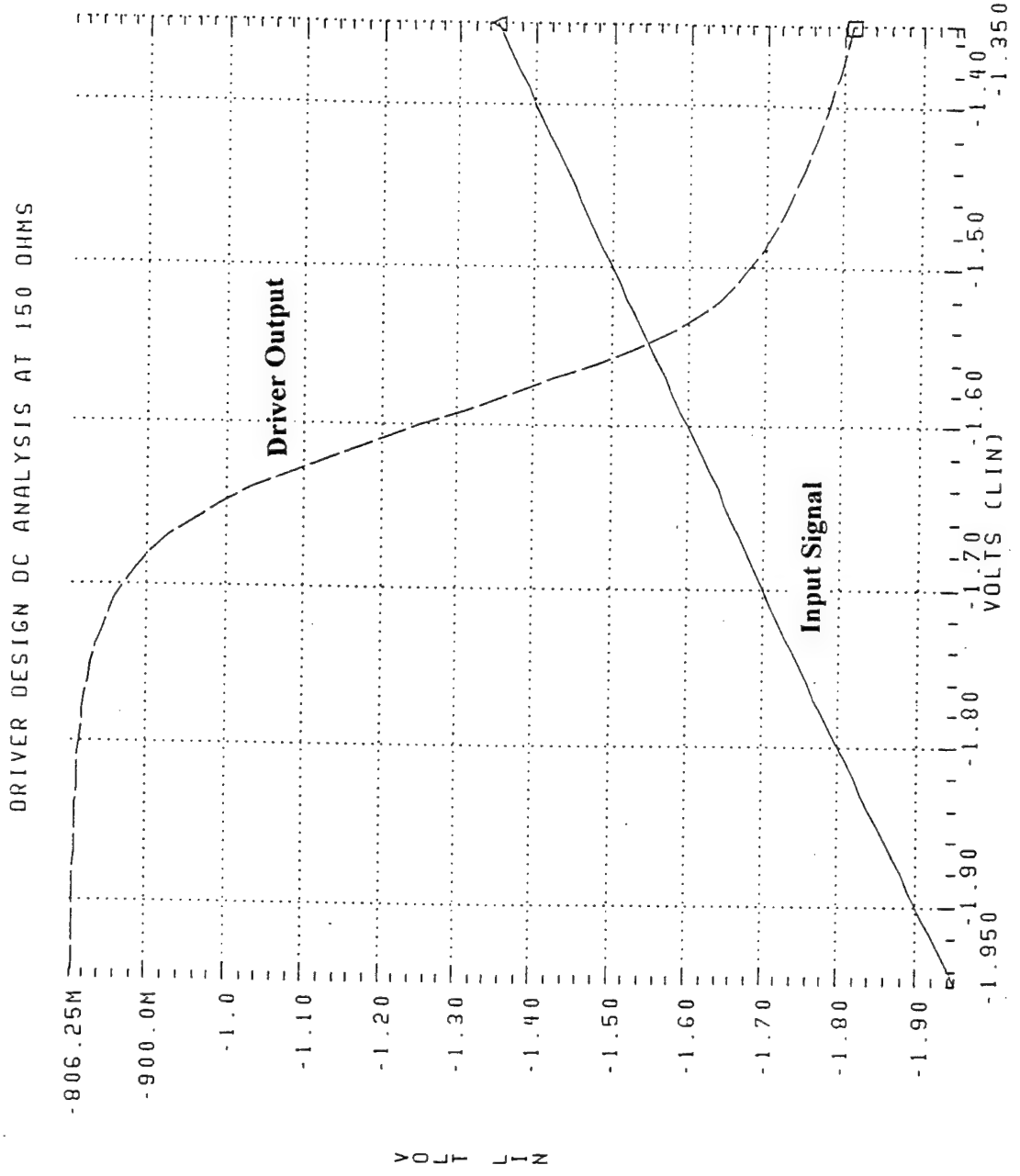

Figure 3-6 DC Analysis of Driver Design for 150-Ohm Load

follower. The change in size of the receiver as the load impedance increased was found to be significant. In Very Large Scale Integrated circuit design (VLSI), transistor area can become a significant factor. The driver results indicate that as impedance is increased, the relative sizes of some transistors in the circuit are significantly reduced. Appendix B contains the HSPICE code used to plot the DC and transient characteristics of the driver.

2. Modeling With Transmission Line Model of the Printed Circuit Board Interconnect

Once the HSPICE models worked at the different impedances, it was important to investigate how the circuits are affected by the printed circuit board and the receiver. Appendix B contains HSPICE code used to incorporate both the driver circuits and their respective PCB interconnect circuits together for both the DC and transient analysis. As was expected, the driver circuit DC runs were not affected by the rest of the interconnect circuits (Figure 3-7 through 3-9). The circuits behaved as they did when run with a load resistor.

The next important step was to test the speed of the circuits and to see how high the frequency could be and still maintain acceptable signals at two places: The terminating resistor and the input to the receiver. All would be lost if the circuit could not drive the receiver to convert the signals back to the on-chip voltages. Figures 3-10 through 3-12 show the transient analysis for driver circuits and interconnect with 50-, 100-, and 150-ohm loads.

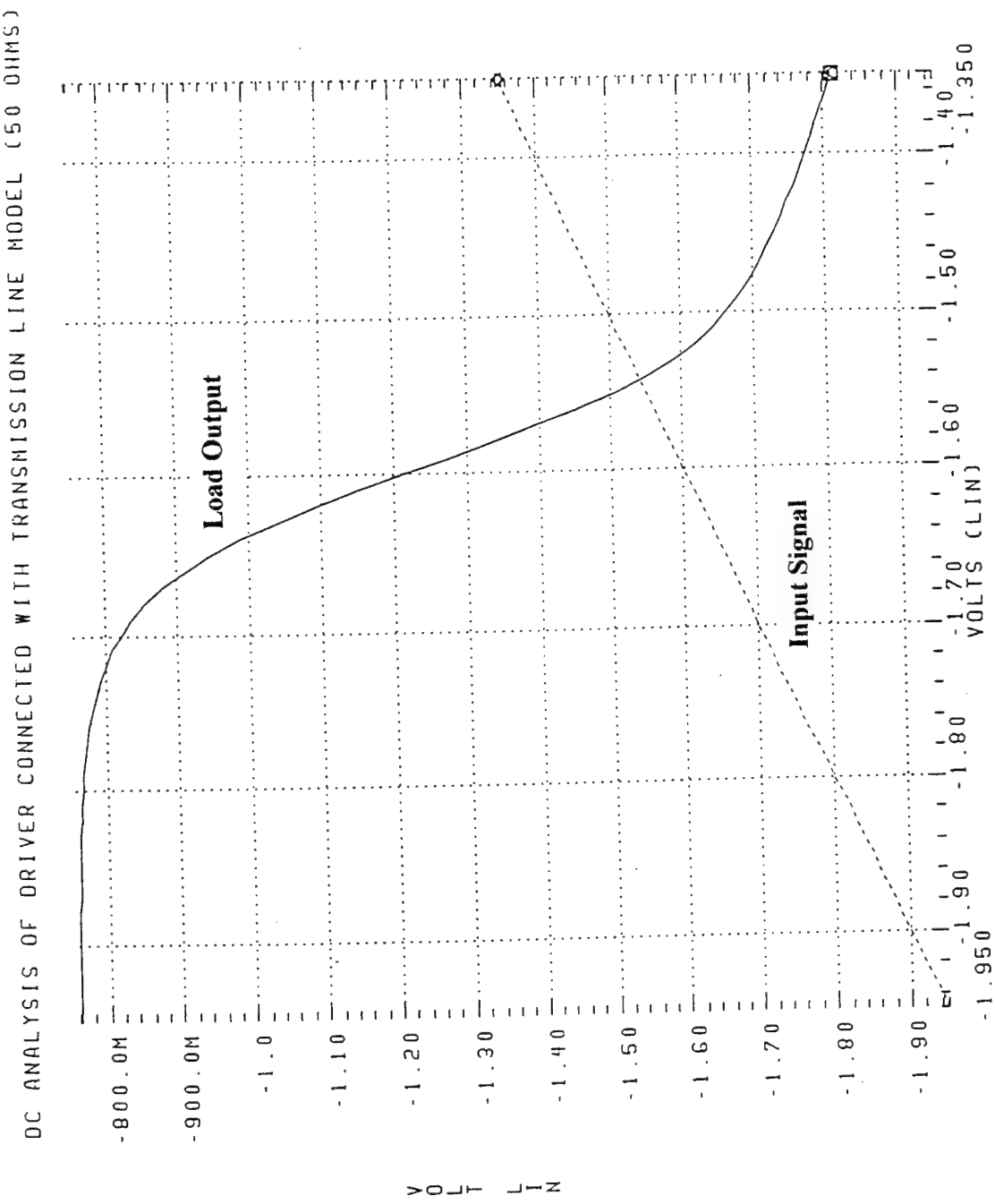

Figure 3-7 DC Analysis of Driver and PCB Interconnect With 50-Ohm Load

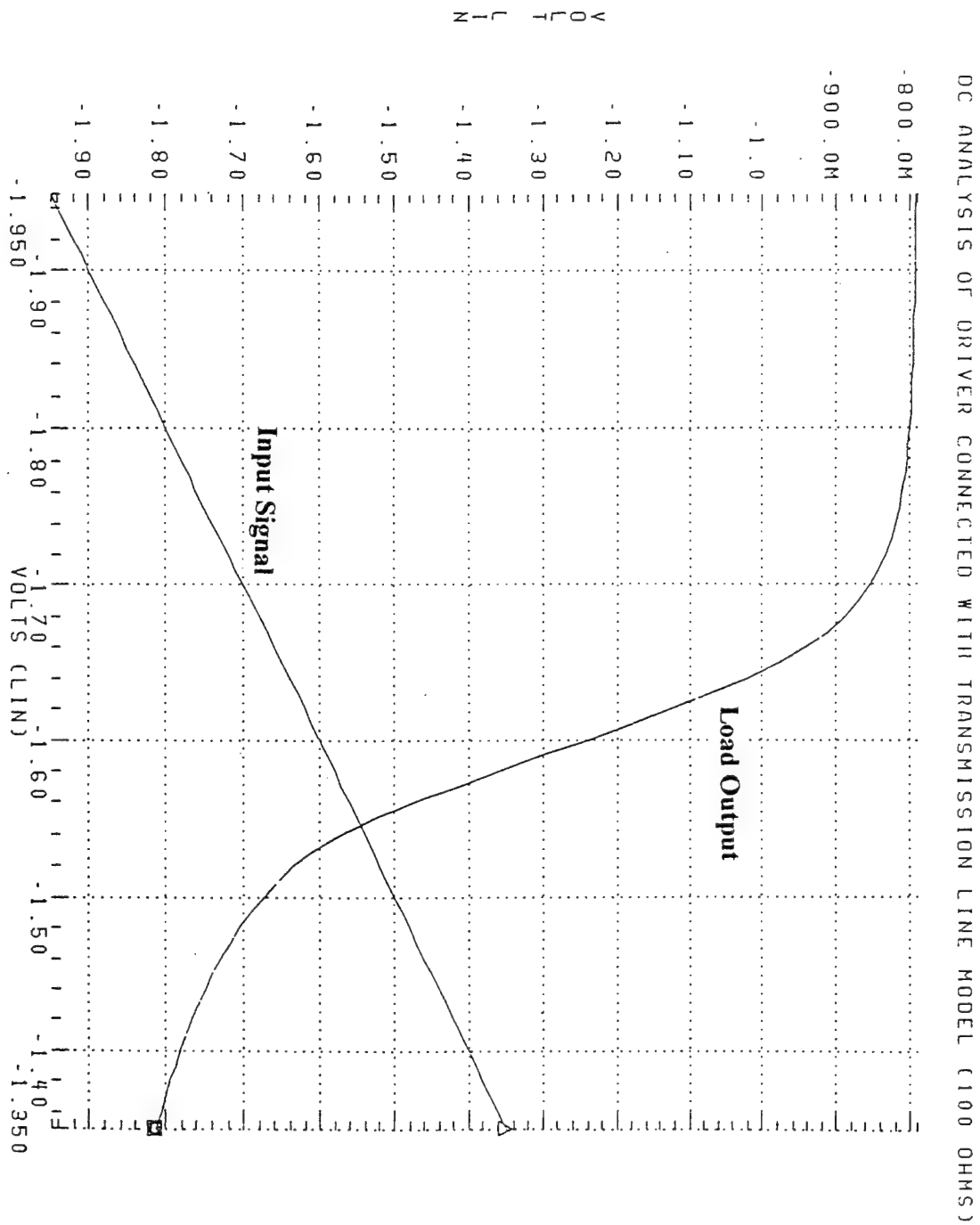

Figure 3-8 DC Analysis of PCB Interconnect and Driver With 100-Ohm Load

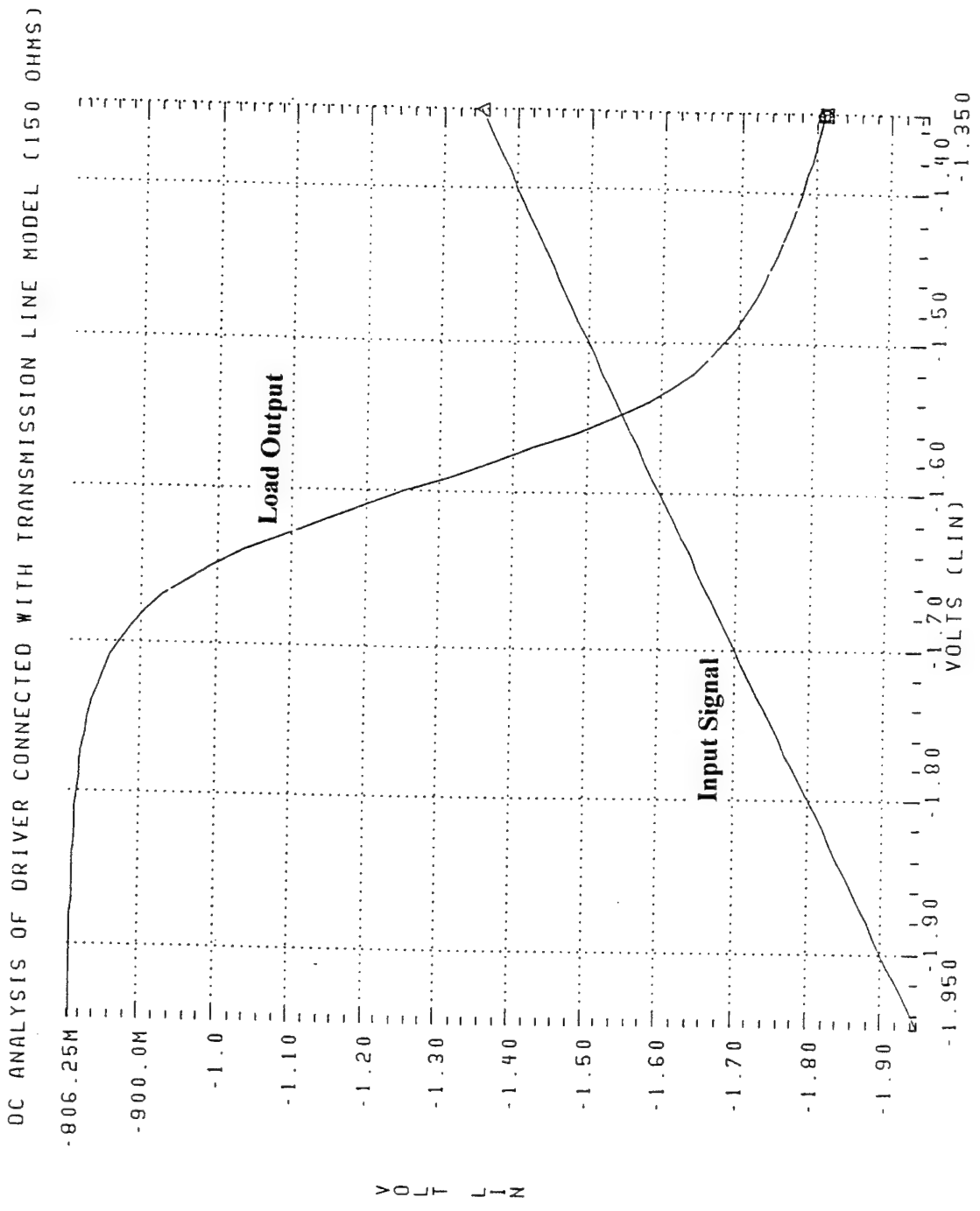

Figure 3-9 DC Analysis of PCB Interconnect and Driver with 150-Ohm Load

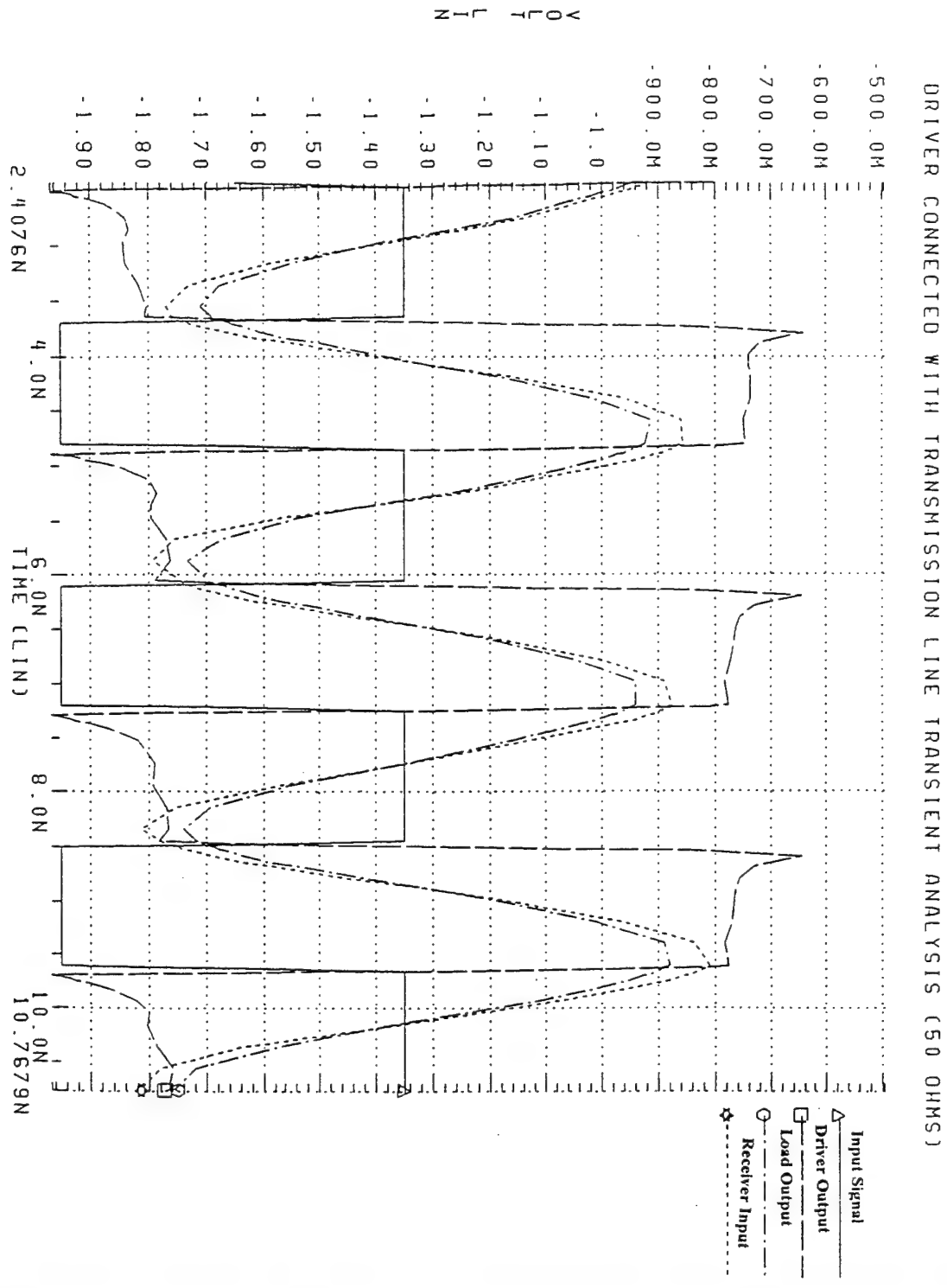

Figure 3-10 Transient Analysis of PCB Interconnect and Driver With 50-Ohm Load

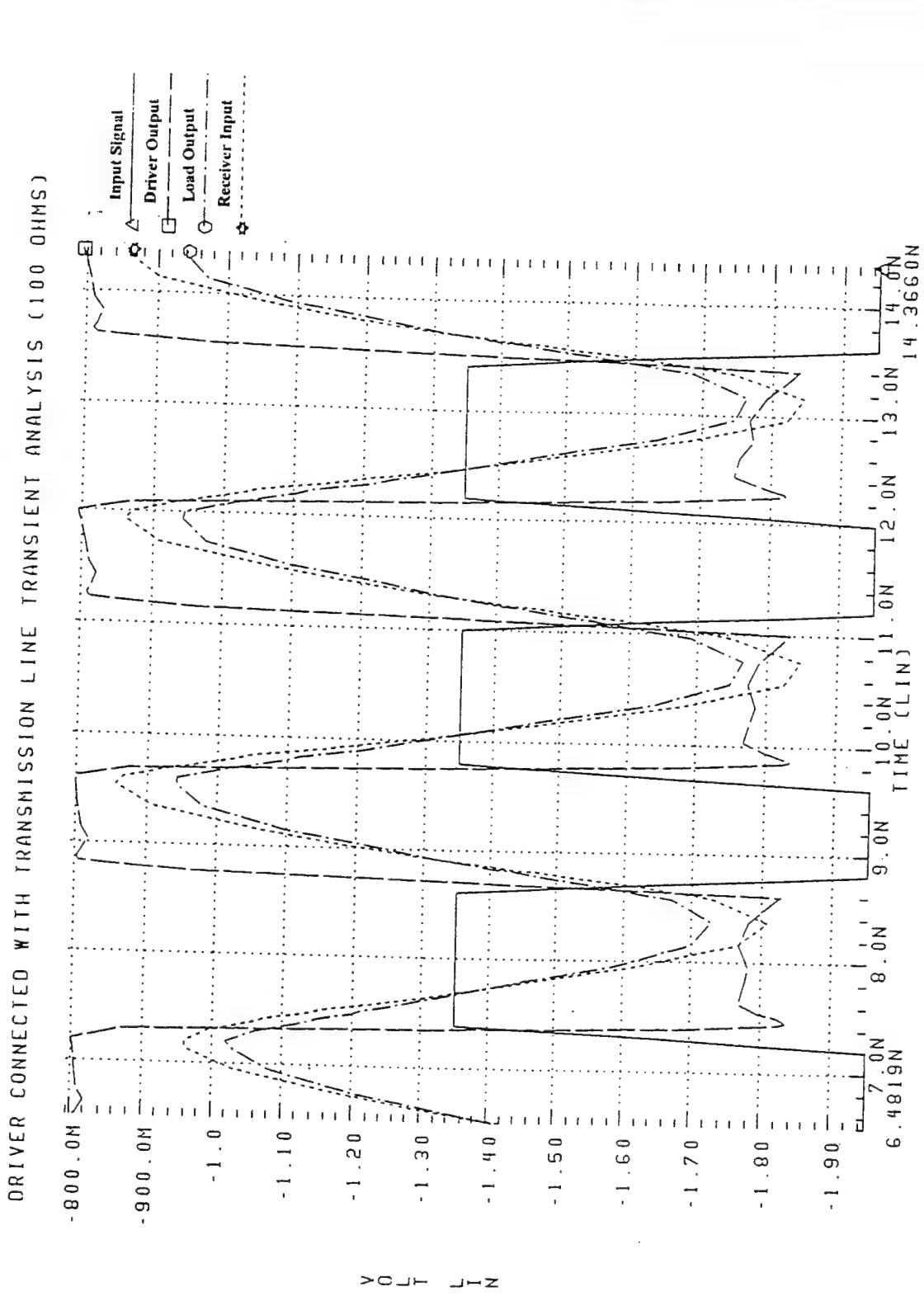

Figure 3-11 Transient Analysis of PCB Interconnect and Driver With 100-Ohm Load

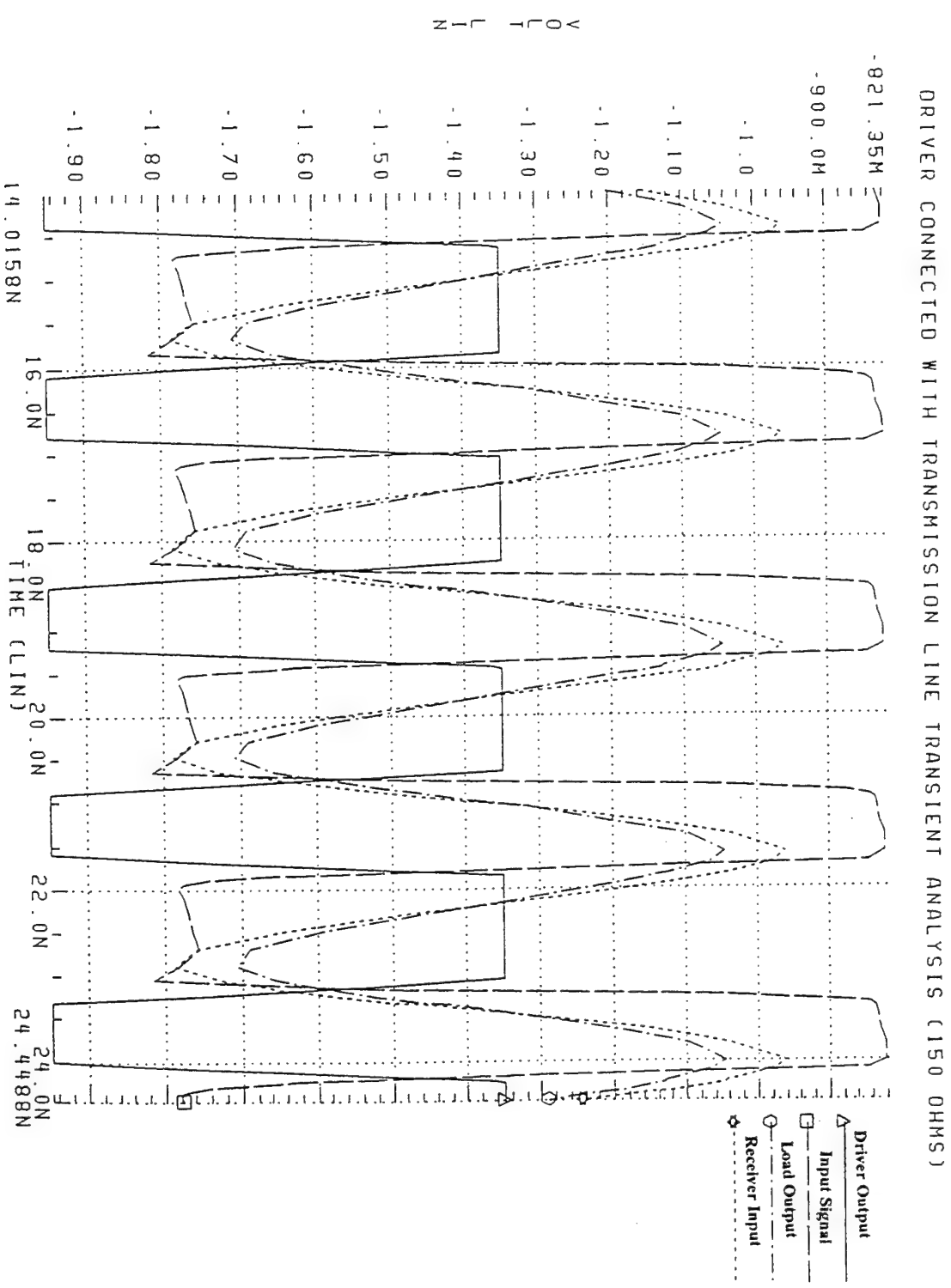

Figure 3-12 Transient Analysis of PCB Interconnect and Driver With 150-Ohm Load

It was found that the circuits all ran at close to the same maximum frequency. All three circuits were able to attain a period of 2.4 nanoseconds. Interconnect impedance was not shown to be a critical limiting factor of speed.

Figure 3-13 shows the difference in source-follower EFET sizes as well as the maximum speed attained at each impedance level. As stated before, the Figure shows the significant difference in gate sizes, while still maintaining the same frequency.

	50 Ohms	100 Ohms	150 Ohms
Source Follower EFET Size	500 microns	200 microns	120 microns
Maximum Speed (Driver with PCB model)	2.4 nanoseconds (417 MHZ)	2.4 nanoseconds (417 MHZ)	2.4 nanoseconds (417 MHZ)

Figure 3-13 Differences in Source Follower EFET Sizes

In this chapter, drivers are developed and simulated. The driver interconnect is found to work well with the printed circuit board. The next step is to design the receiver interconnect and simulate the design in HSPICE to ensure that the interconnect maintains a reasonably high speed as well as the proper voltages.

IV. GALLIUM ARSENIDE RECEIVER DESIGN

A. RECEIVER CHARACTERISTICS

The receiver is the interface between the PCB and the on-chip circuitry (Figure 3-1). The receiver must have a high input impedance to keep it from loading down the output driver. The receiver also shapes the signal prior to entering the chip logic. The receiver converts the off-chip voltages, which range from -0.8 volts to -1.8 volts, to on-chip voltages, which are -1.35 volts to -1.95 volts. The output impedance of the receiver is usually low. Since the input impedance of the driver must be high, the assumption was that one receiver design would be acceptable to all three interconnect impedance levels.

B. CIRCUIT DESIGN OF GALLIUM ARSENIDE RECEIVER

The principle behind the design of the receiver is similar to the design of the driver. The high input impedance of the input to the receiver is accomplished with a source-follower buffer. The output from the buffer must be stepped down to a reasonable voltage swing. Inverters were used to step down the voltage swing. Initially, there was no way of knowing how many invertors were going to be needed to accomplish the goal. The initial design assumed at least three invertors in cascade would be required. Diodes were also considered if there was a requirement to drop the voltage down by 0.6 volts or more.

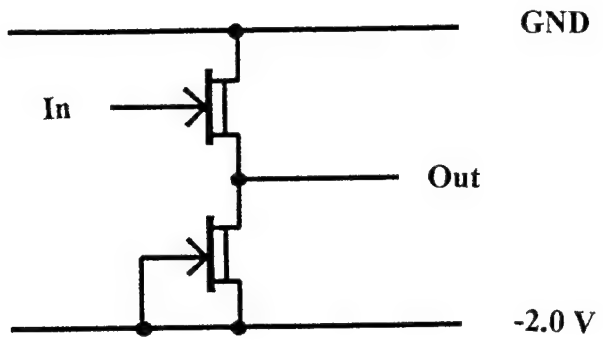

Figure 4-1 Source-Follower Buffer Design

C. HSPICE MODELING OF RECEIVER

1. Standalone Modeling

The design of the receiver relied on creating the source-follower buffer, then creating the inverters, followed by a superbuffer (Figure 3-2) output stage. The first step was to design a HSPICE DC model of the receiver. Appendix C contains the HSPICE code for the DC and transient models of the receiver. The final circuit required a buffer, followed by 3 stages of inverters, all of which were connected to a superbuffer. The superbuffer was used on the receiver output because the receiver might have to drive long on-chip interconnect lines between the receiver output and the input to the "core" logic of the chip.

Figure 4-3 shows the DC analysis of the circuit. Unlike the driver circuit, large transistors were not necessary. The receiver could rely on smaller, faster transistors to do the work. As a result, the receiver was expected to be faster than the driver.

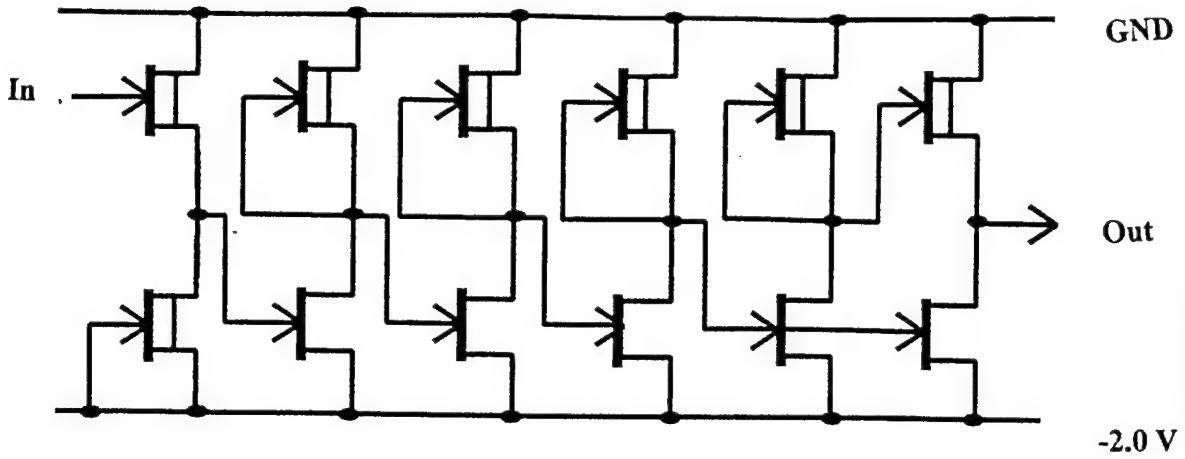

Figure 4-2 Receiver Design

After designing an appropriate DC model of the receiver and finding that all the parameters were met, the next step was to see how the system worked at high speed using transient analysis. Appendix C contains the HSPICE code required to perform the transient analysis. Figure 4-4 shows the final transient analysis output of the receiver. As expected, the receiver worked well and met all voltage specifications. It was found to have a maximum speed of 1 gigahertz (GHZ).

2. Modeling With Transmission Line Model of Printed Circuit Board Interconnect.

There were two major concerns when connecting the receiver to the driver and interconnect circuits. The first one was ensuring that the receiver did not excessively load down the driver. The second was to ensure that the driver could drive the receiver and swing from voltage low to high and vice versa. Appendix C contains the HSPICE

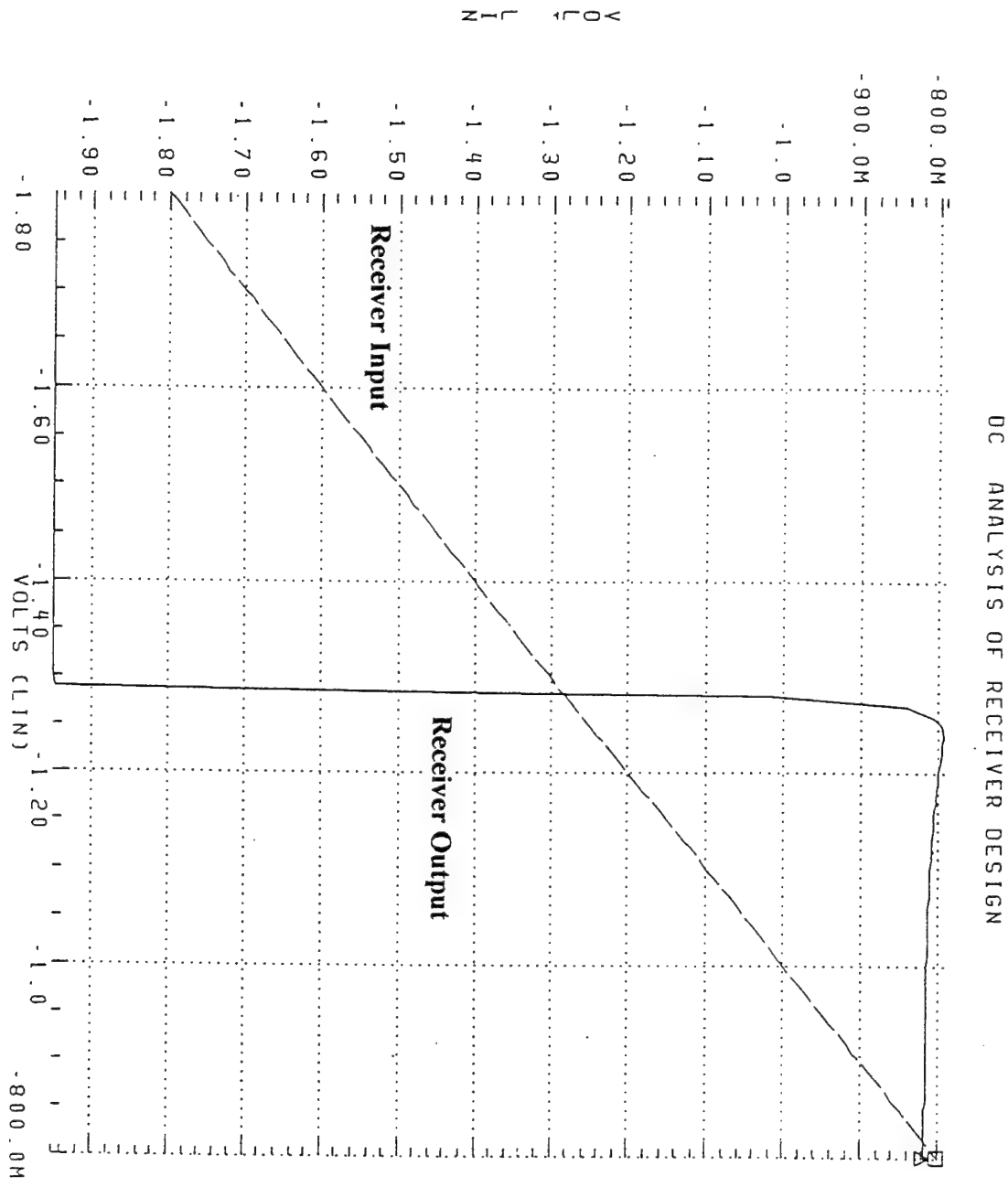

Figure 4-3 DC Analysis of Receiver Design

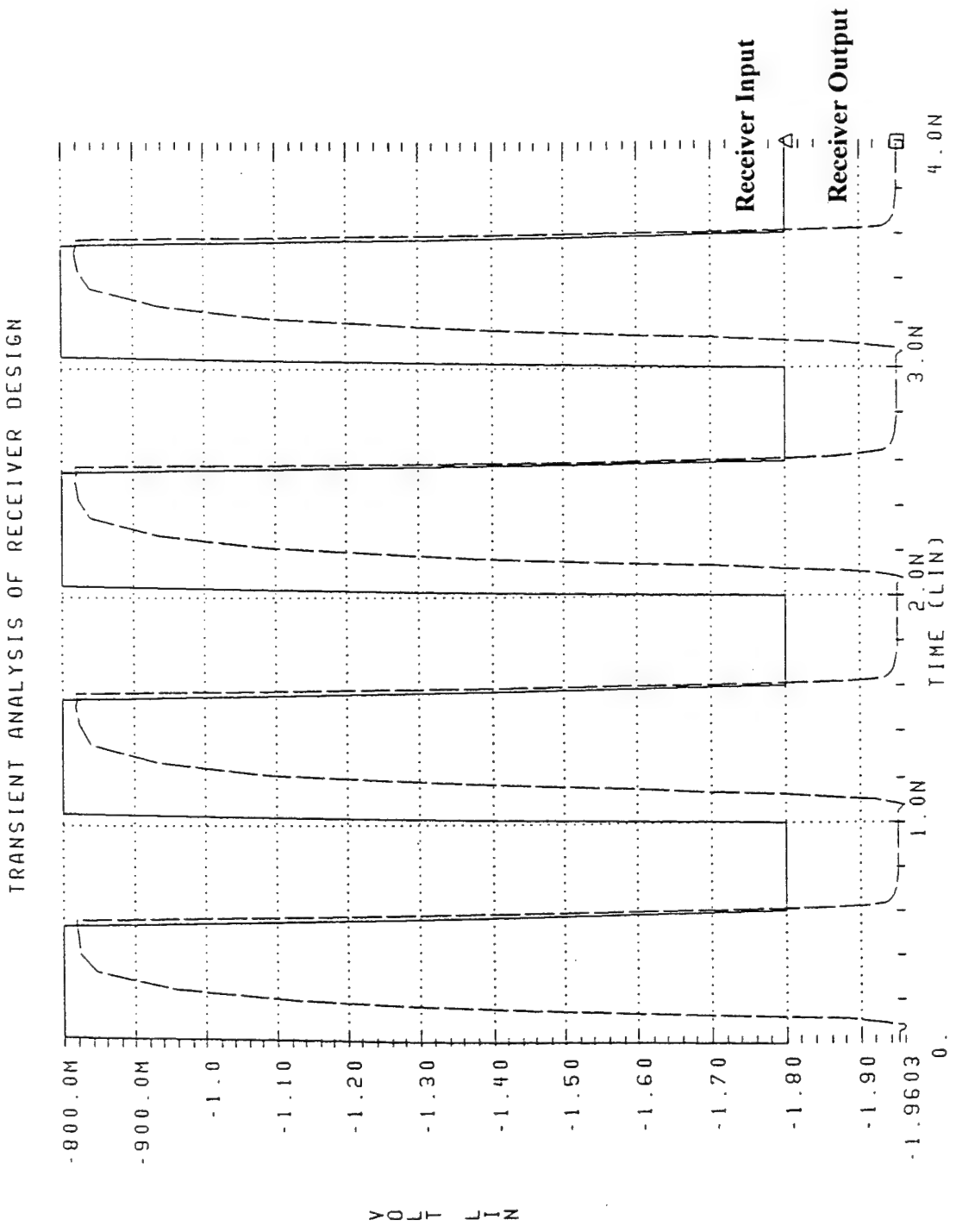

Figure 4-4 Transient Analysis of Receiver Design

code for this portion of testing. The receiver was tested with all three driver/interconnect circuits. The results showed that there was no change in the output of the receiver when connected to any of the three different driver/interconnect circuits.

3. Modeling With Driver and Printed Circuit Board Interconnect

Once the models of all three parts of the circuit worked properly alone, the next step was to connect them all together. The first goal was to find out if all worked together within voltage parameters. The second goal was to determine the maximum speed for all three impedance levels, to prove that the change in impedance either enhanced the maximum speed or was negligible. The final goal was to determine the power consumption of these circuits at high speeds to prove that increasing the characteristic impedance of the PCB interconnect and load termination did,in fact, reduce power consumption. Appendix C contains the HSPICE code for all three simulations on the three complete circuits. HSPICE confirmed that all three complete circuits worked well.

Figures 4-5 through 4-13 display the transient analysis at each different impedance level. The graphs are an indication of the maximum speeds that can be attained with the driver and receiver circuits created. In the 50-ohm model, the maximum speed attained before the voltage at the load resistor fell below -1.7 volts was 2.2 nanoseconds, or 455 MHZ (Figure 4-7). The voltage at the load resistor is the limiting factor in the speed of the circuit because this is the voltage seen by the receiver. In the 100-ohm model, the speed was found to be 2.3 nanoseconds, or 435 MHZ

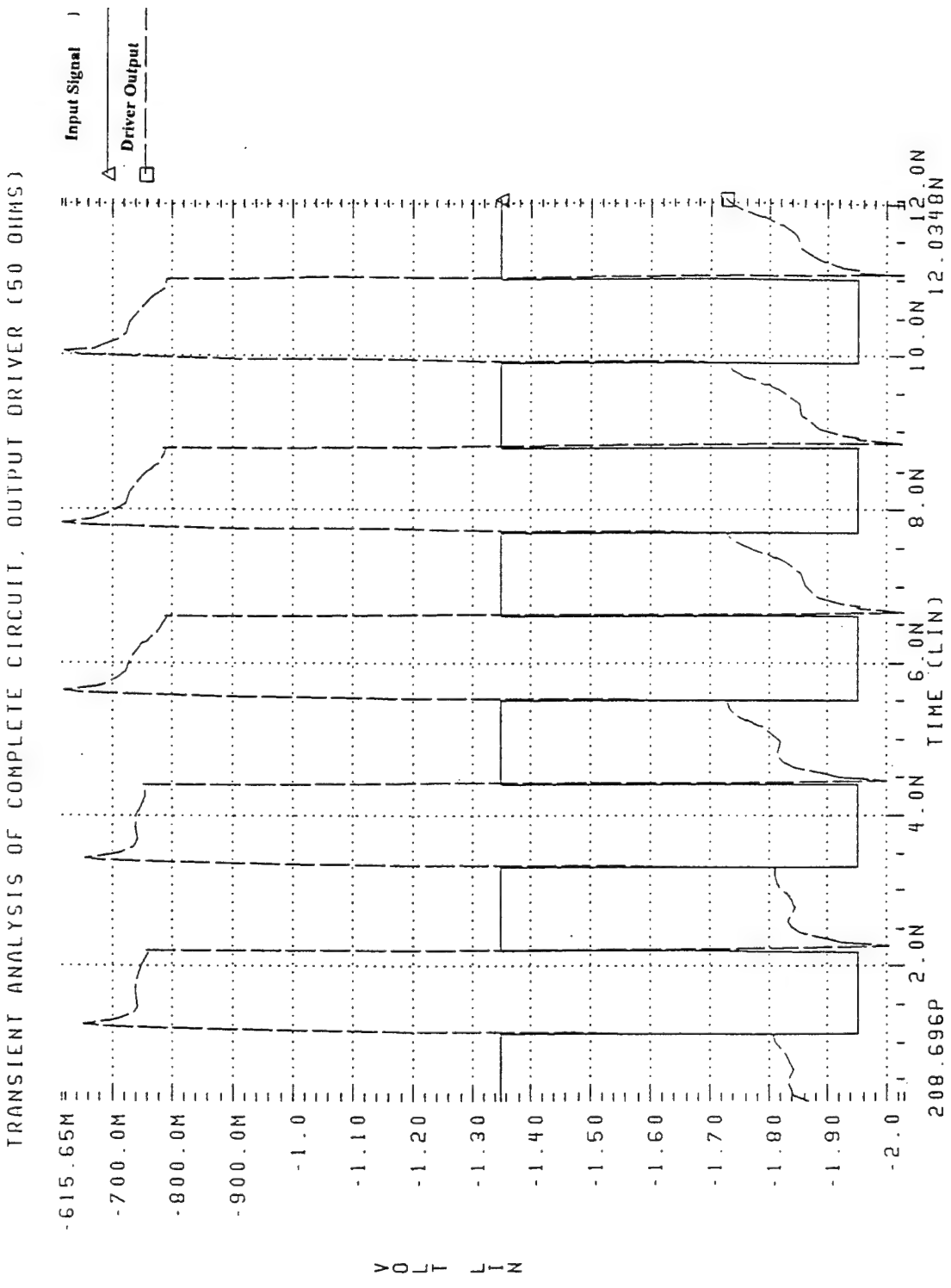

Figure 4-5 Transient Analysis of Complete Circuit With 50-Ohm Interconnect

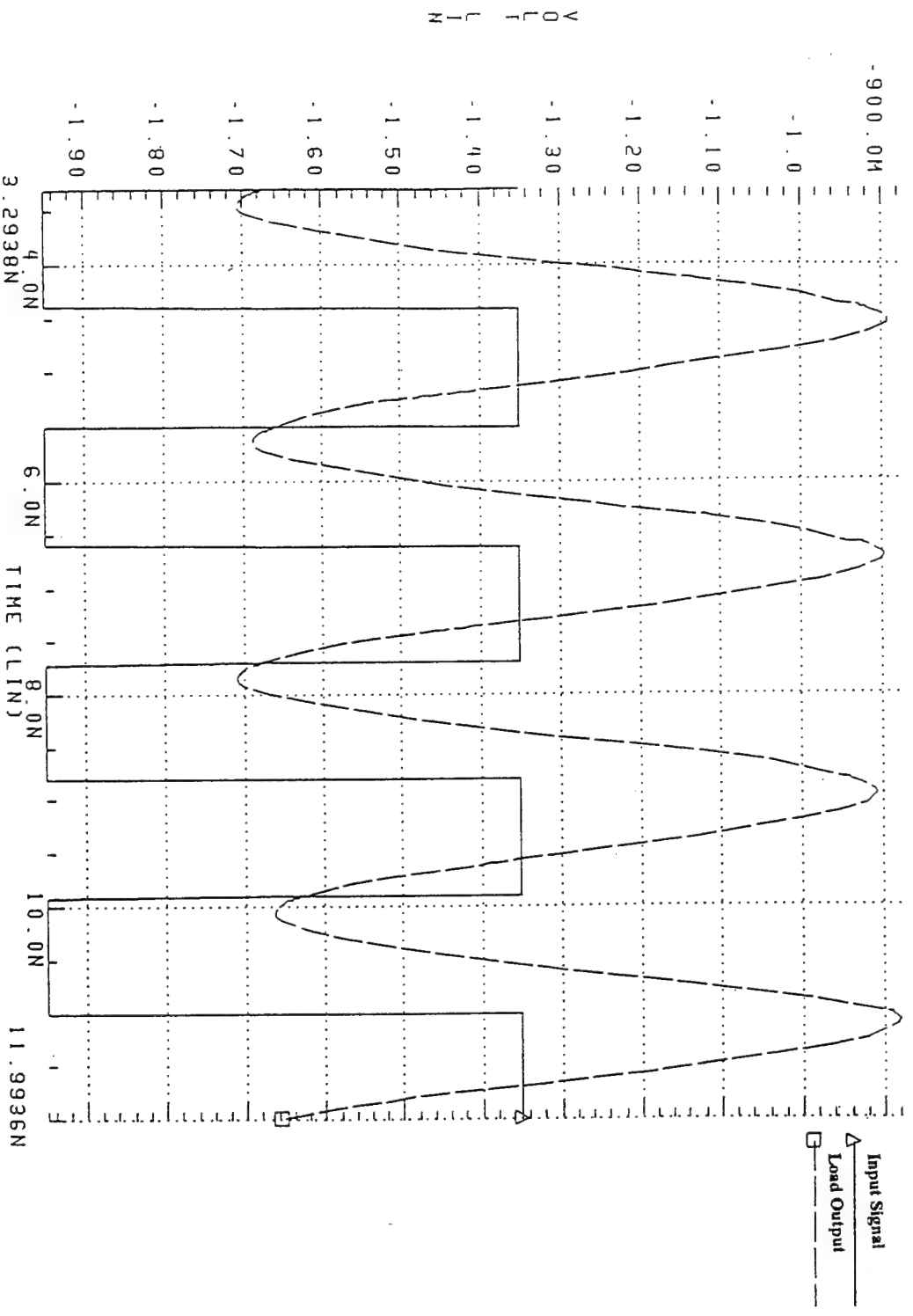

Figure 4-6 Transient Analysis of Complete Circuit With 50-Ohm Interconnect

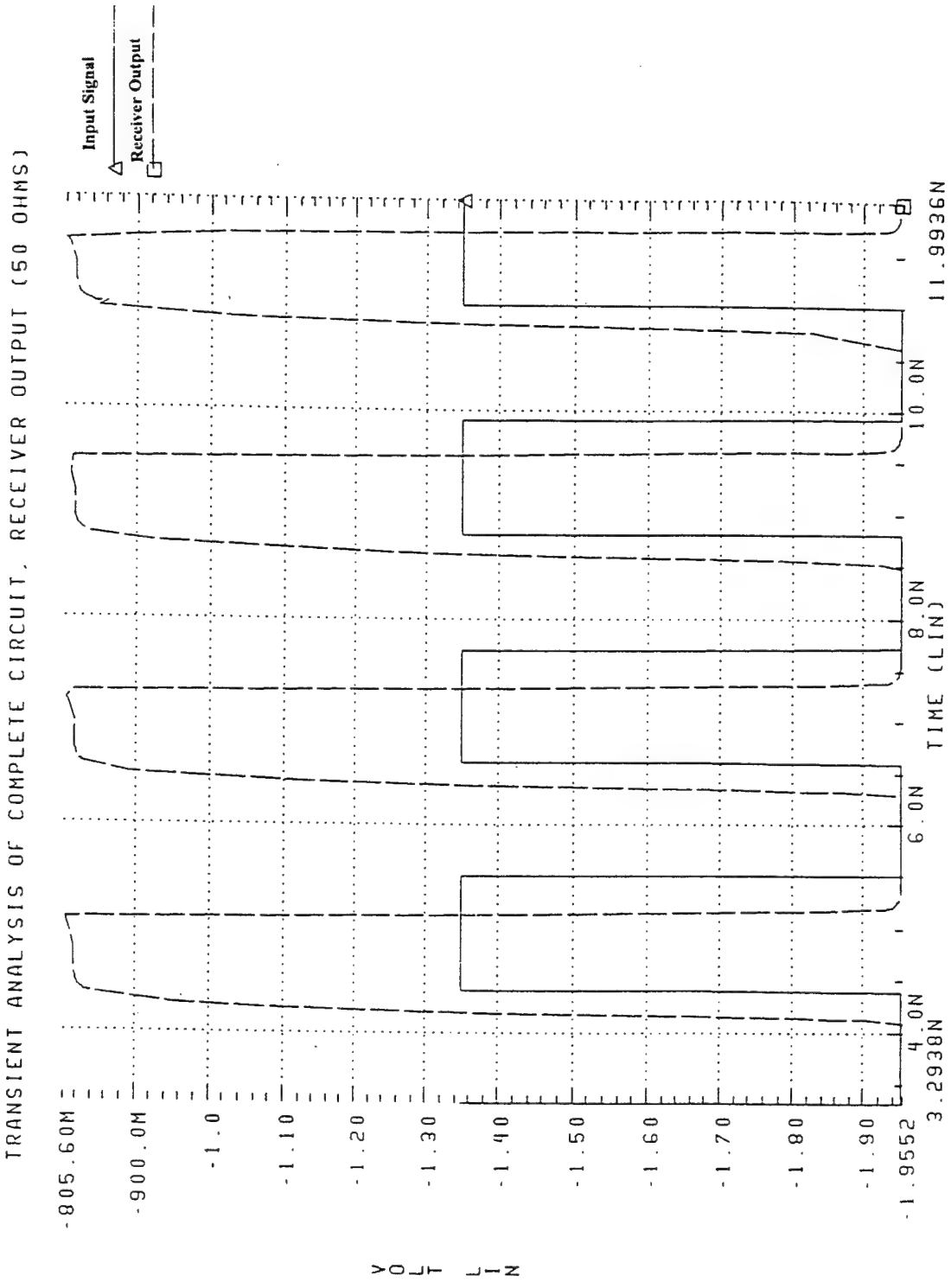

Figure 4-7 Transient Analysis of Complete Circuit With 50-Ohm Interconnect

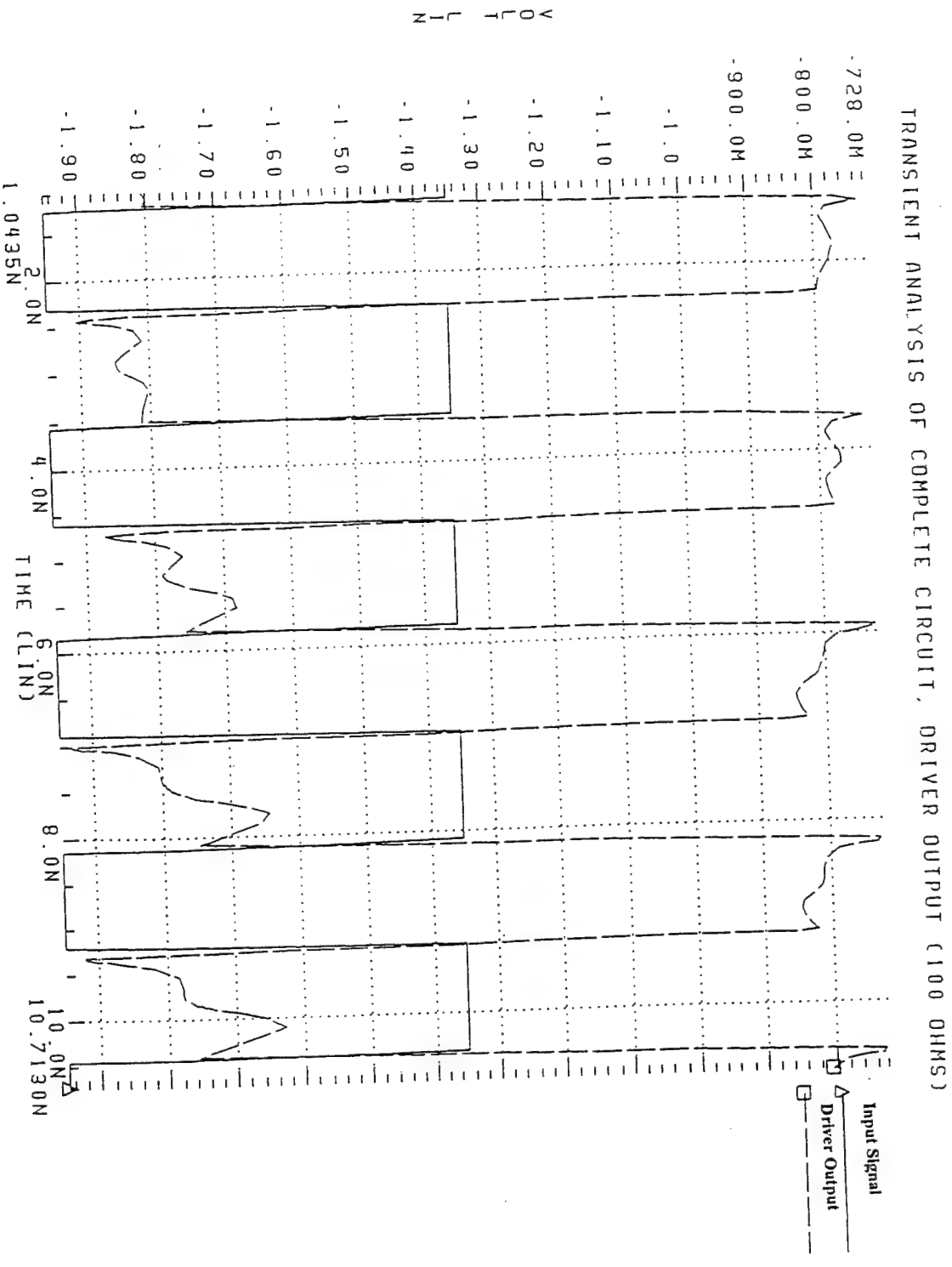

Figure 4-8 Transient Analysis of Complete Circuit With 100-Ohm Interconnect

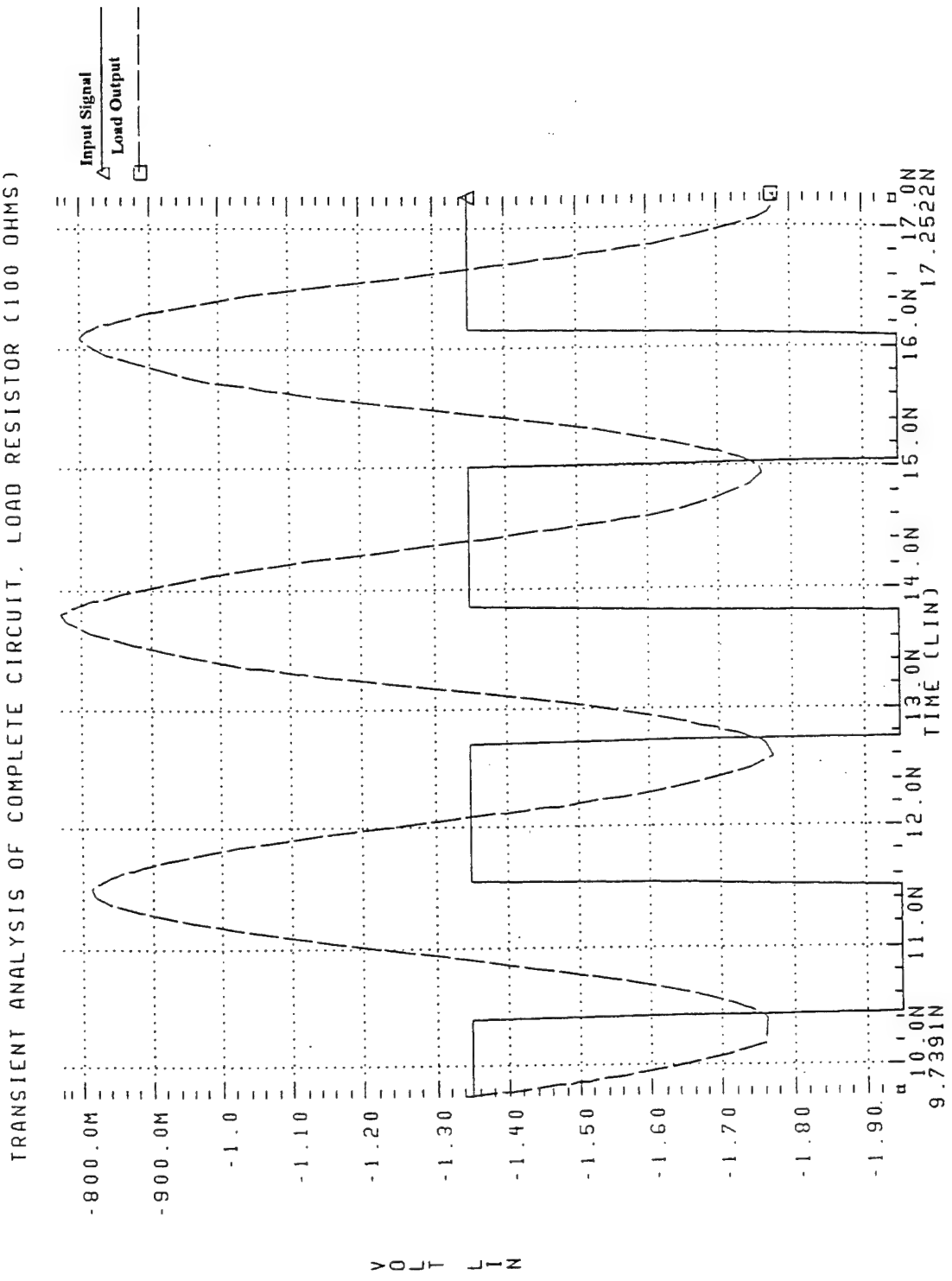

Figure 4-9 Transient Analysis of Complete Circuit With 100-Ohm Interconnect

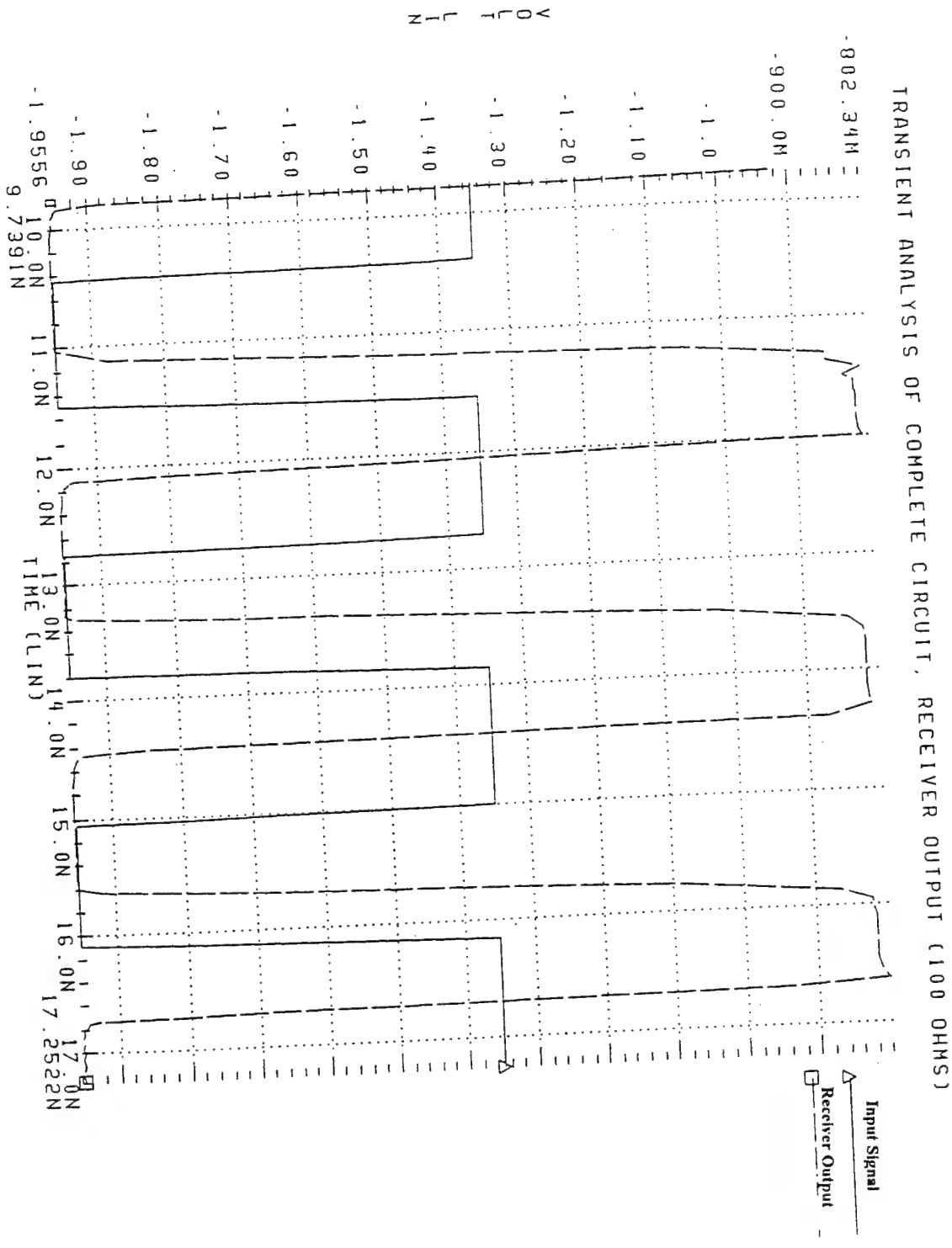

Figure 4-10 Transient Analysis of Complete Circuit With 100-Ohm Interconnect

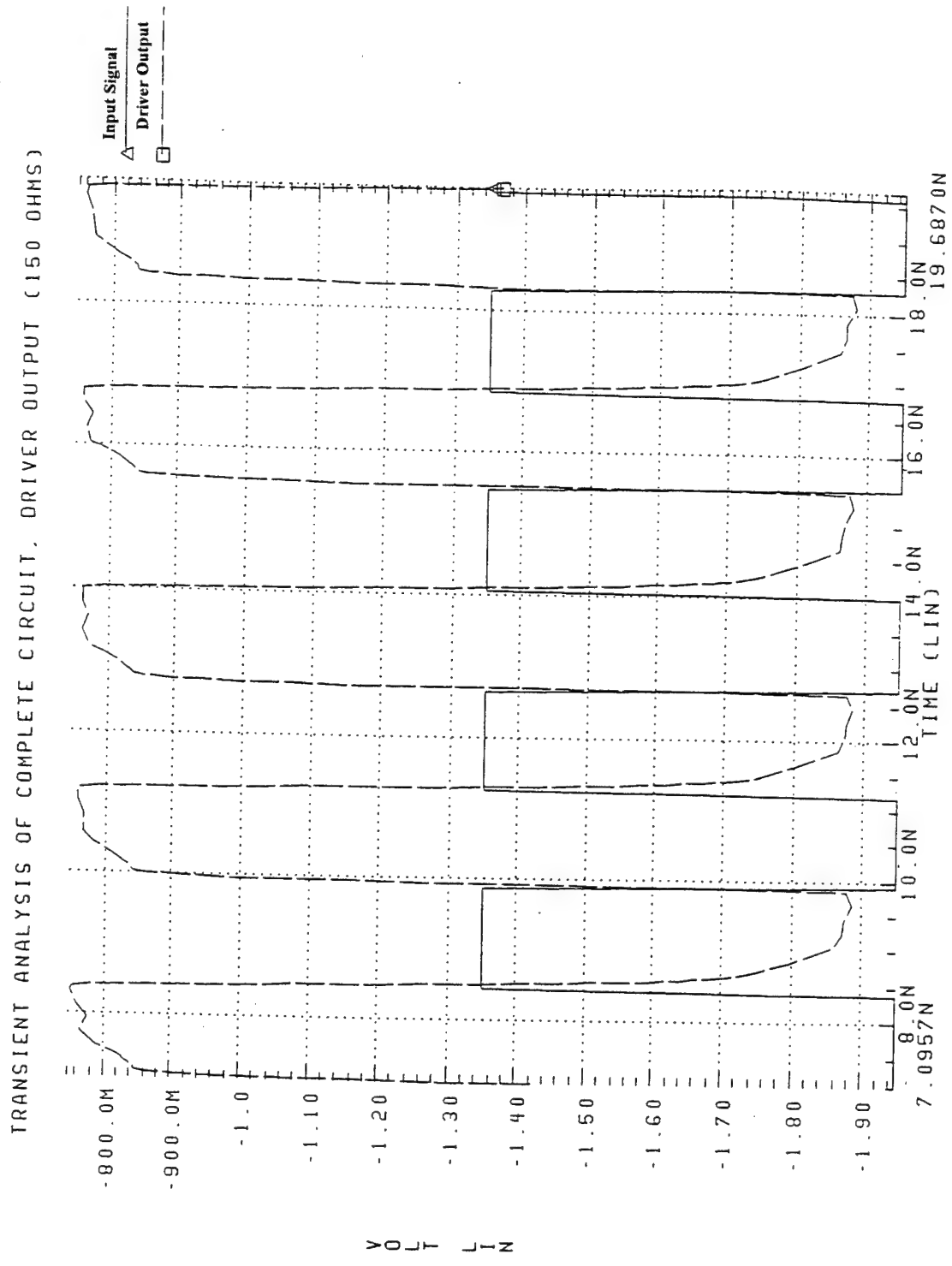

Figure 4-11 Transient Analysis of Complete Circuit With 150-Ohm Interconnect

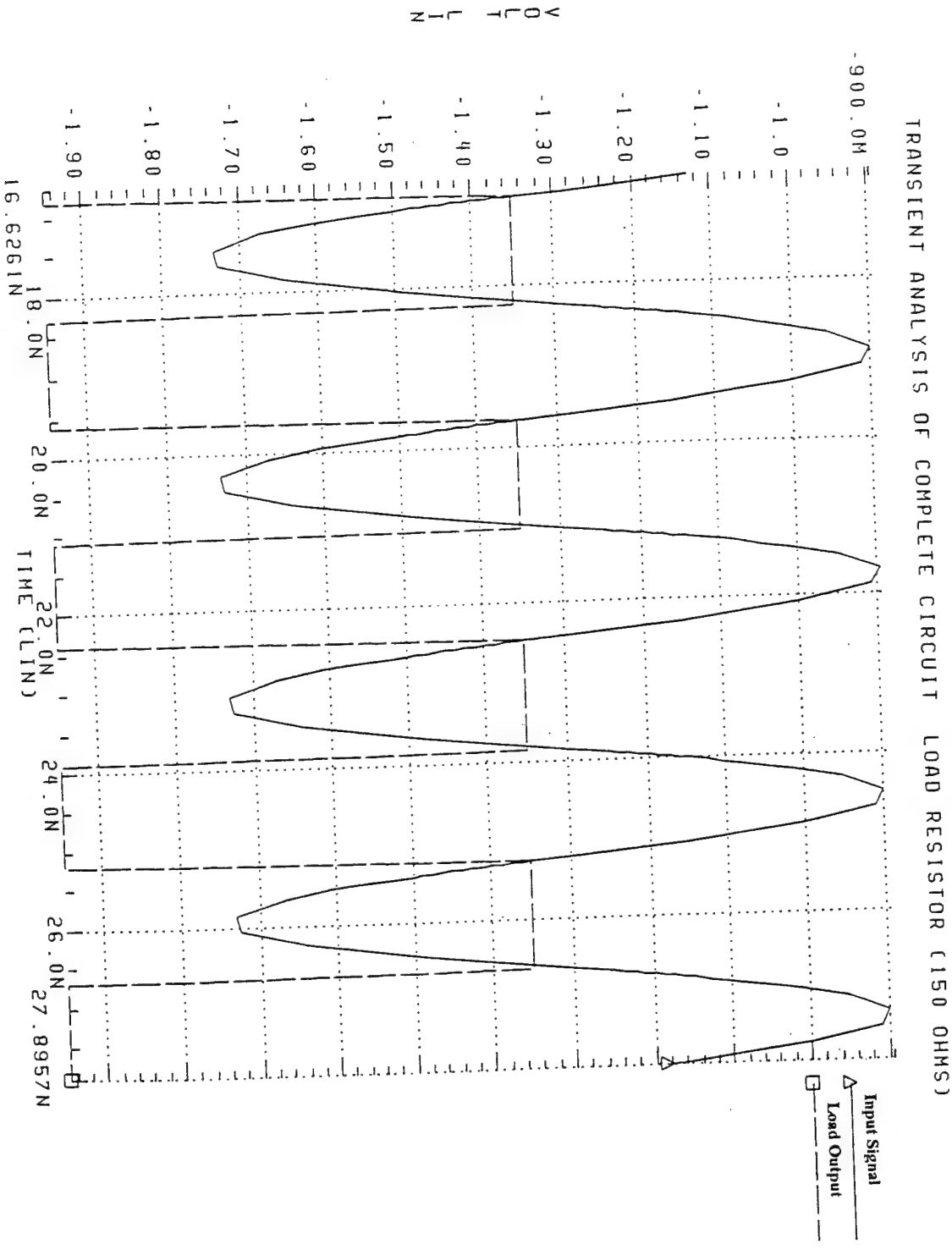

Figure 4-12 Transient Analysis of Complete Circuit With 150-Ohm Interconnect

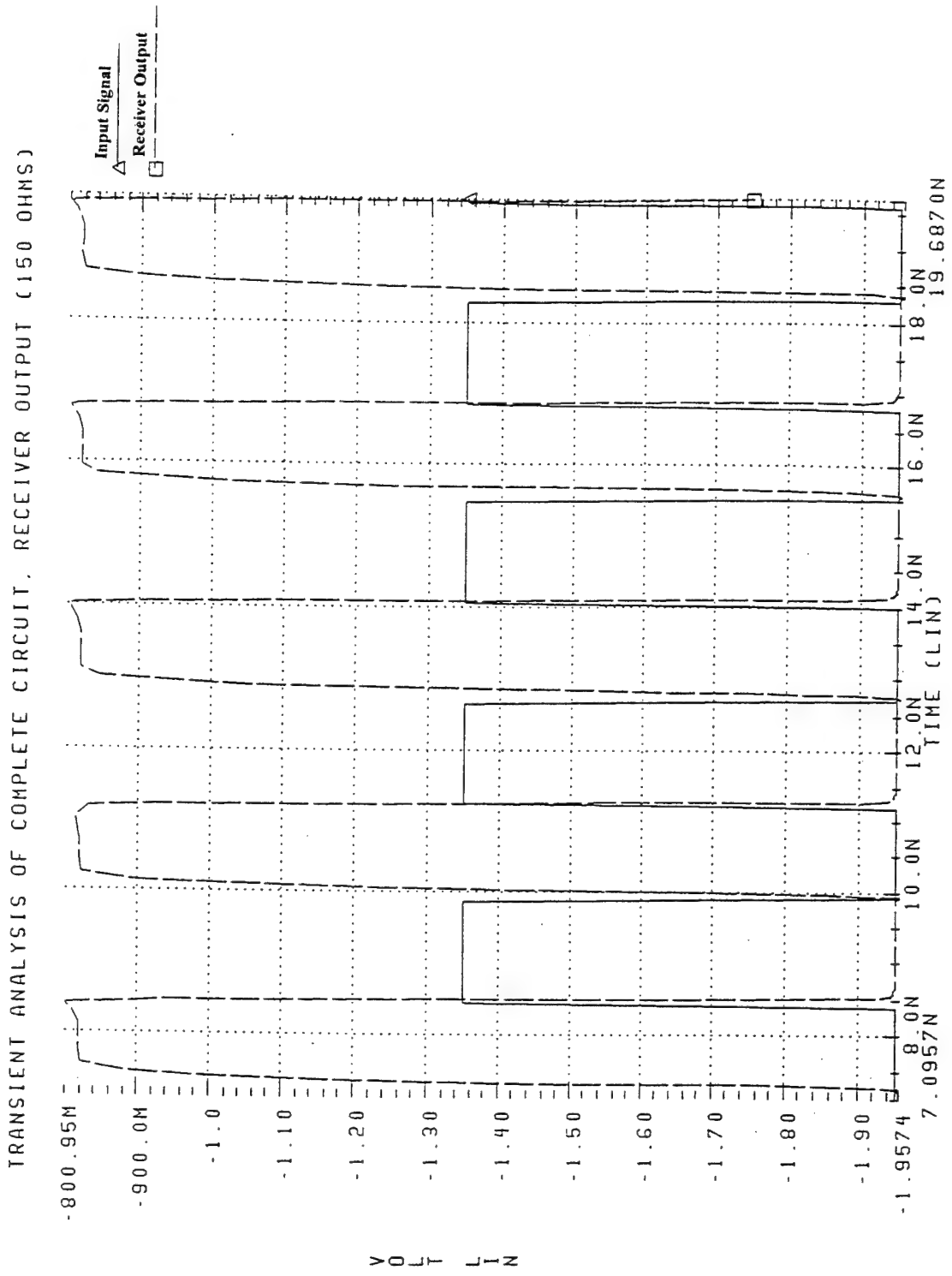

Figure 4-13 Transient Analysis of Complete Circuit With 150-Ohm Interconnect

(Figure 4-10). The 150-ohm model was the slowest, with a speed of 2.8 nanoseconds, or 357 MHZ (Figure 4-13). These differences provided significant insight into the effects of higher impedance interconnects. As the impedance grew, the speed decreased. The reason for the difference in the speeds was attributed to the RC time constants of the interconnect. The decrease in the capacitance in the drivers at each impedance level was not as significant as the increase in the RC time constant as interconnect and termination impedance increased. Figure 4-14 tabulates the results found in the HSPICE modeling. There is a 4.4 percent loss in frequency when the impedance of the interconnect was increased to 100 ohms. There is an even greater loss in frequency of 21.54 percent when the interconnect impedance reaches 150 ohms.

Characteristic Impedance	Maximum Frequency	Percent Difference With 50 Ohms
50 Ohms	455 MHZ	0
100 Ohms	435 MHZ	- 4.40
150 Ohms	357 MHZ	-21.54

Figure 4-14 Overall Comparison of Maximum Circuit Speed

The next consideration to look at was I/O power consumption. The main goal was to reduce power consumption by increasing the characteristic impedance of the interconnect and the termination load. Figures 4-16 through 4-18 show DC power consumption for each circuit from 50- to 150-ohms. Figures 4-19 through 4-21 show the transient power consumption for all three layouts. The data collected from Figure 4-16 to

4-21 can be found in Figure 4-15.

As Figure 4-15 indicates, the assumptions were right. The 50-ohm model ranges from 60 milliwatts to 35 milliwatts, averaging 47 milliwatts of power. The 100-ohm model ranges from 34 milliwatts to 24 milliwatts, averaging 30 milliwatts of power. The 150-ohm model ranges from 21.5 milliwatts to 28 milliwatts, averaging a power consumption of 25 milliwatts. As expected, there is a significant decrease in power as the impedance goes up. In the transient modeling, a similar trend was found. In the 50-ohm model, the power peaked at 100 milliwatts. In the 100-ohm model, this peak was around 55 milliwatts, and in the 150-ohm model, the peak was at 35 milliwatts.

	50 Ohms	100 Ohms	150 Ohms
DC Power Max	60 mW	35 mW	28 mW
DC Power Min	35 mW	24 mW	21.5 mW
Average DC Power	45 mW	30 mW	25 mW
AC Power Max	100 mW	55 mW	35 mW
AC Power Min	20 mW	15 mW	16 mW

Figure 4-15 Power Consumption Overview

This chapter took the entire design and simulated it in HSPICE to determine the speed and power characteristics. The next question to be answered is the difference in sizes between the different impedance designs. The next chapter discusses the design of the driver at each impedance in HSPICE and the differences in their size.

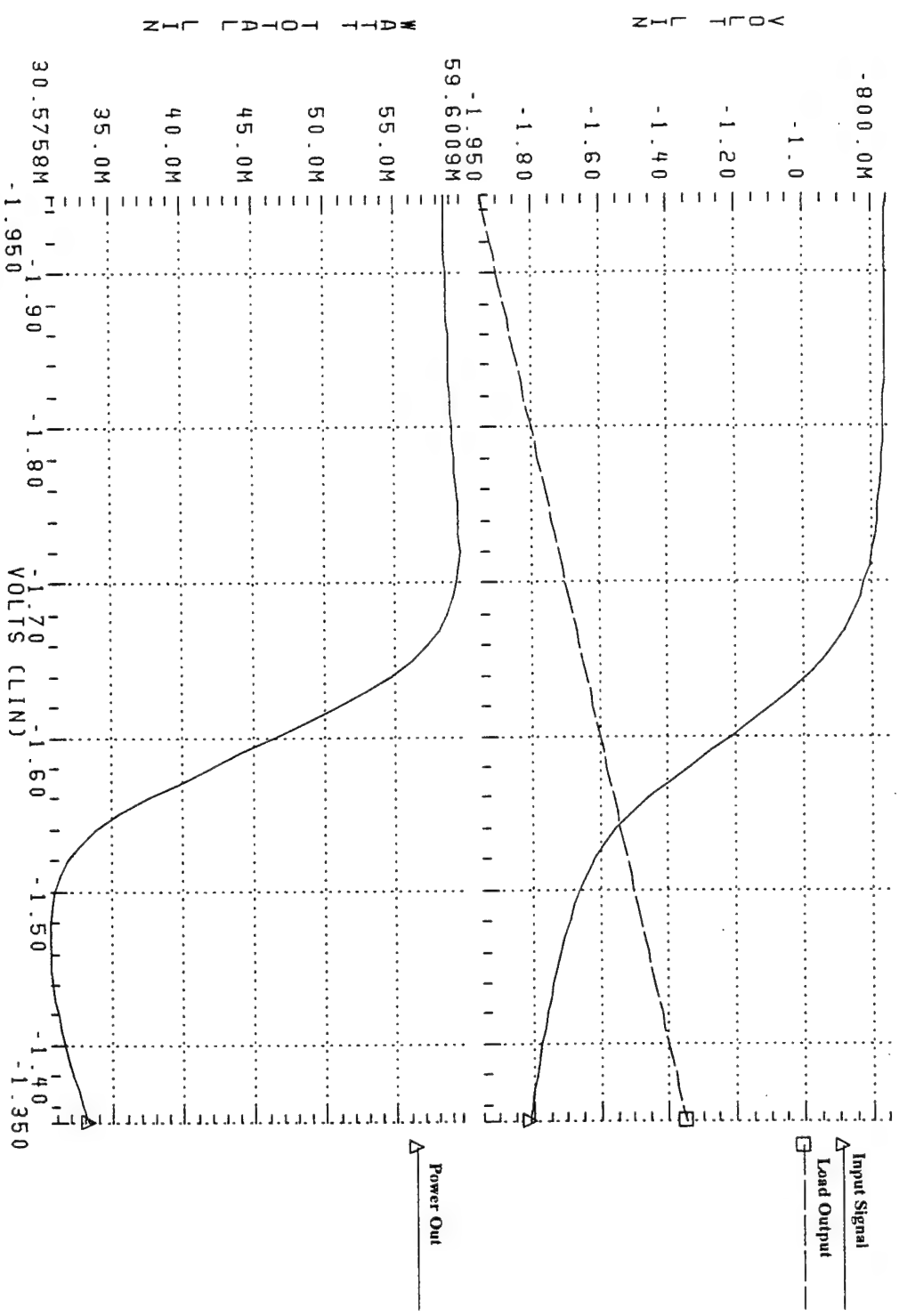

Figure 4-16 DC Power Analysis of Complete Circuit (50 Ohms)

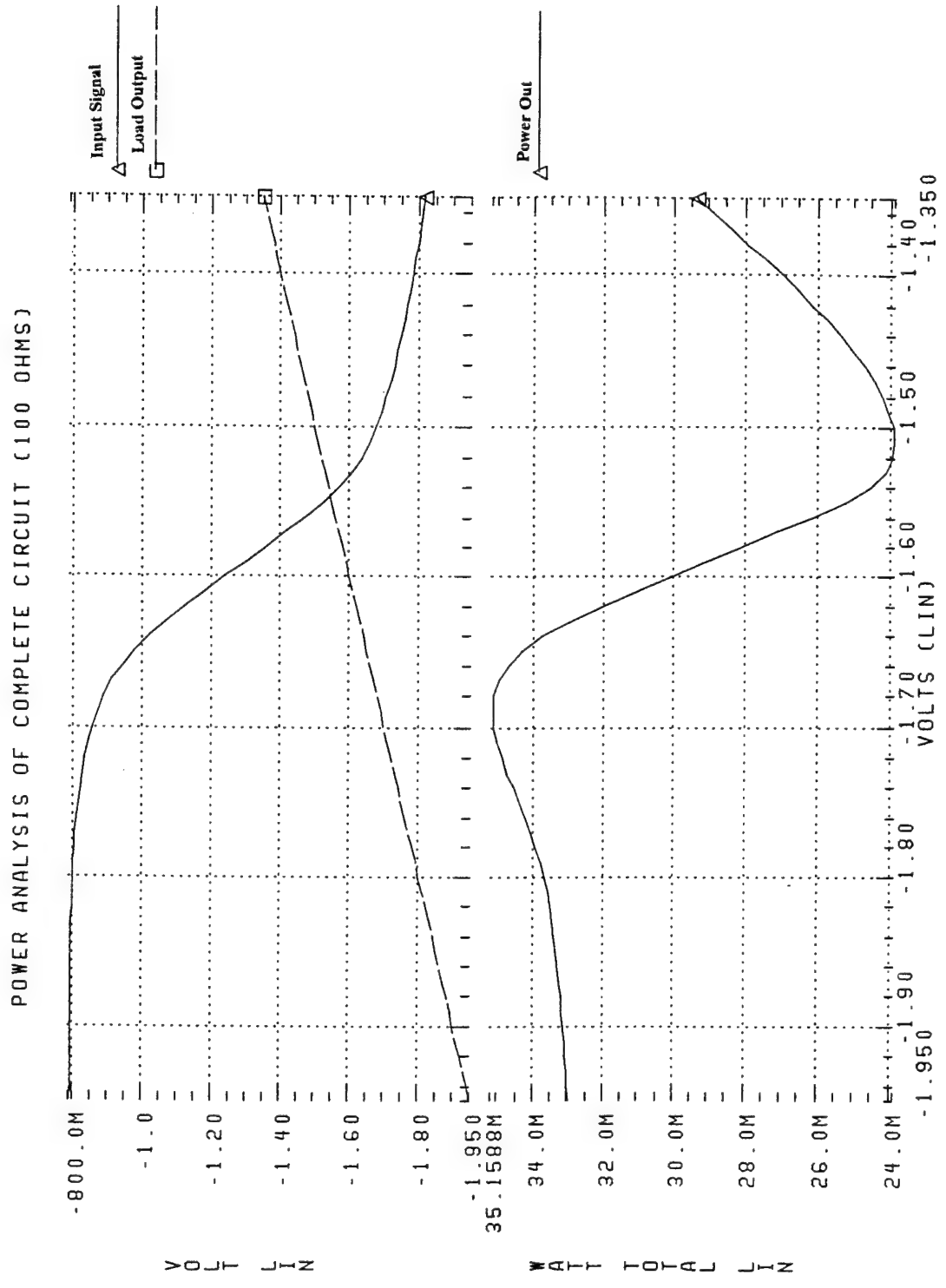

Figure 4-17 DC Power Analysis of Complete Circuit (100 Ohms)

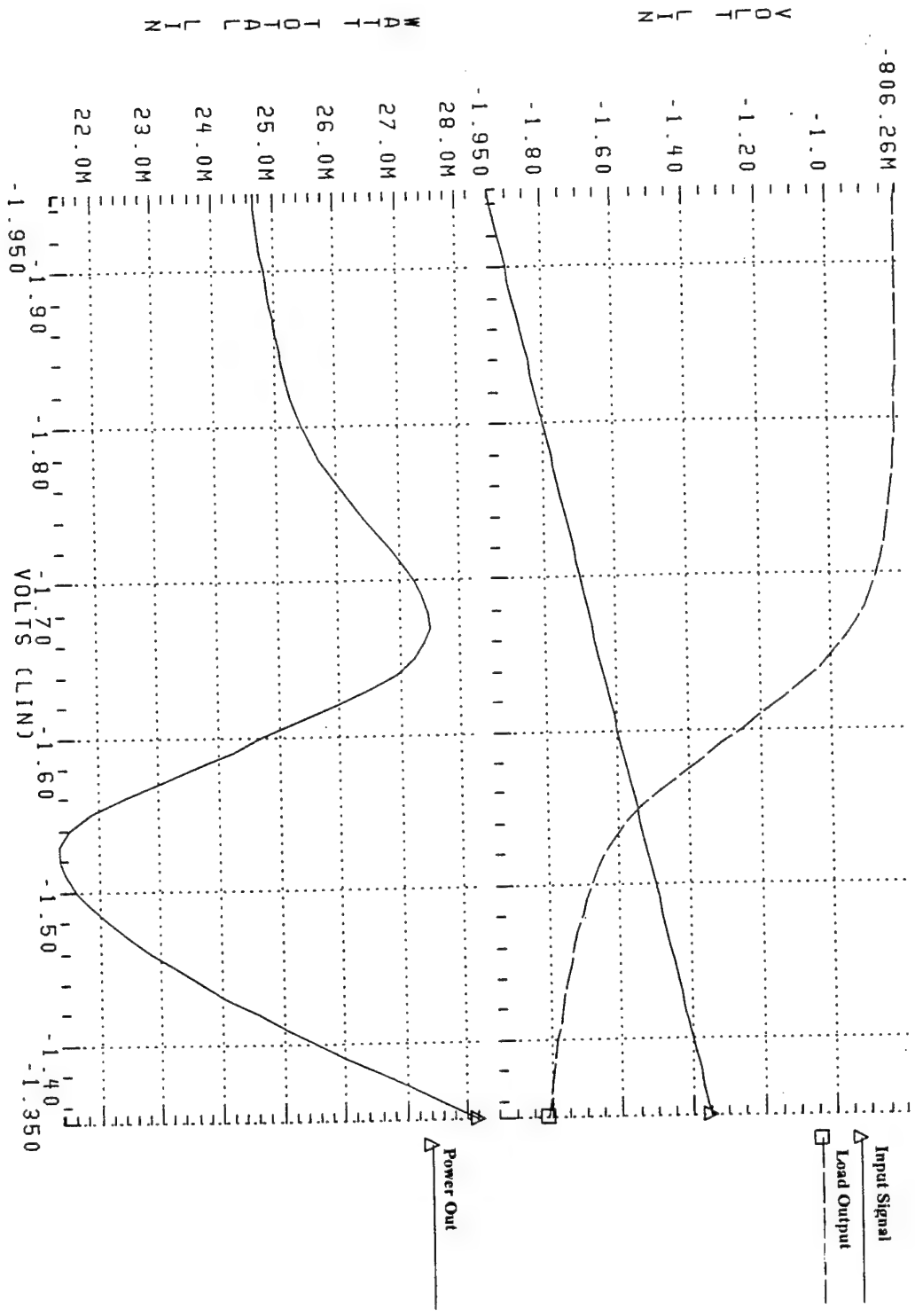

Figure 4-18 DC Power Analysis of Complete Circuit (150 Ohms)

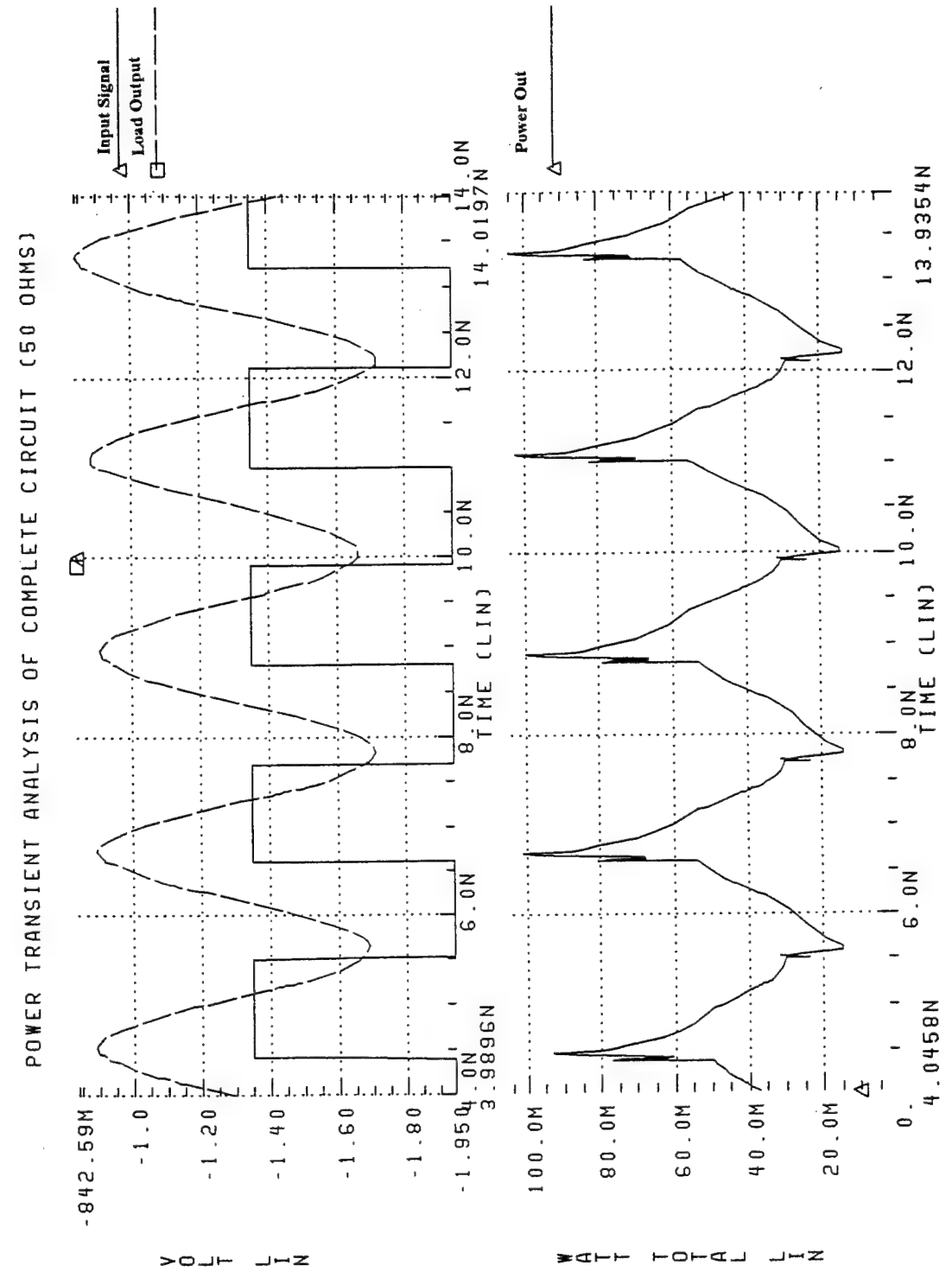

Figure 4-19 Transient Power Analysis of Complete Circuit (150 Ohms)

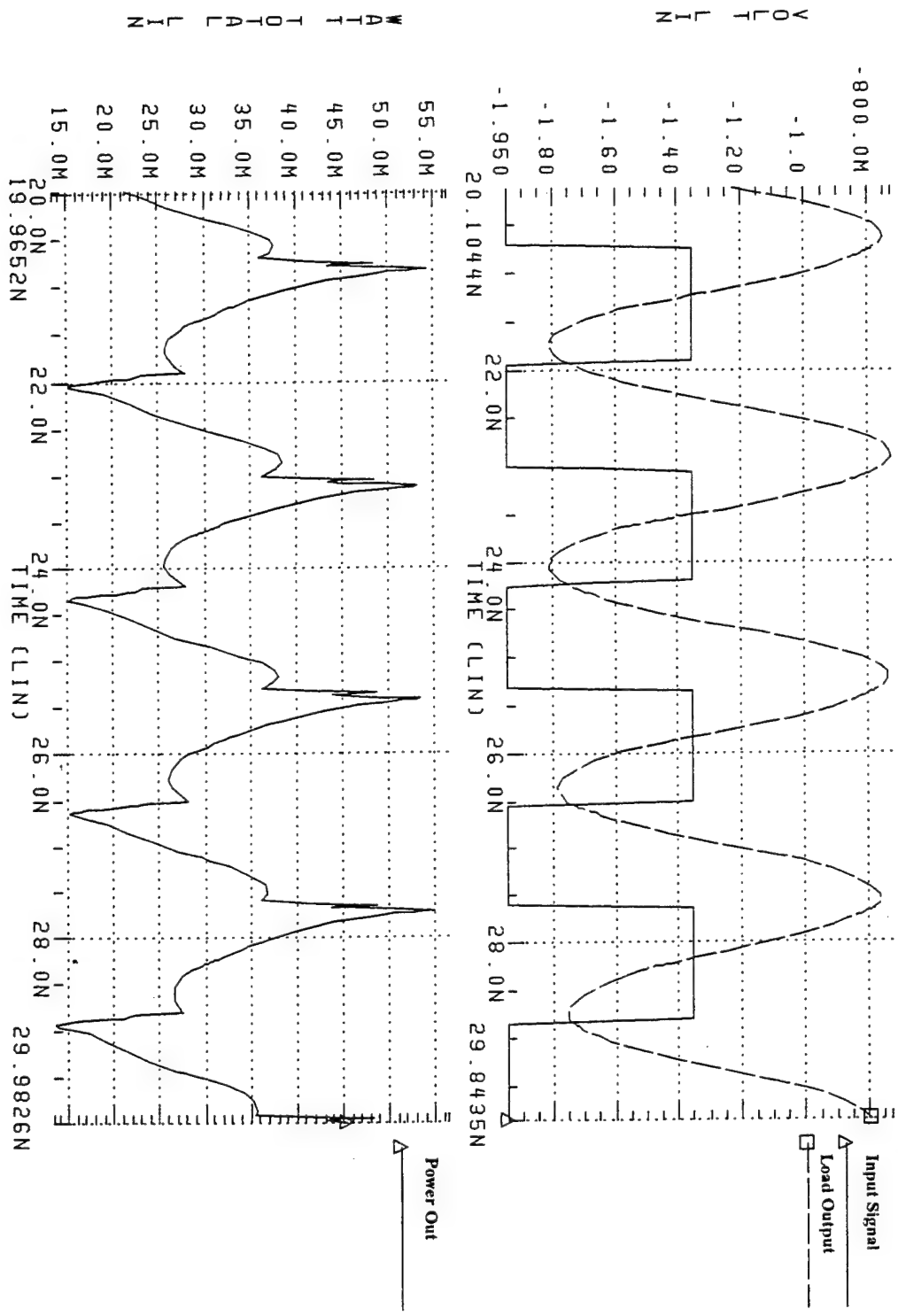

Figure 4-20 Transient Analysis of Complete Circuit (100 Ohms)

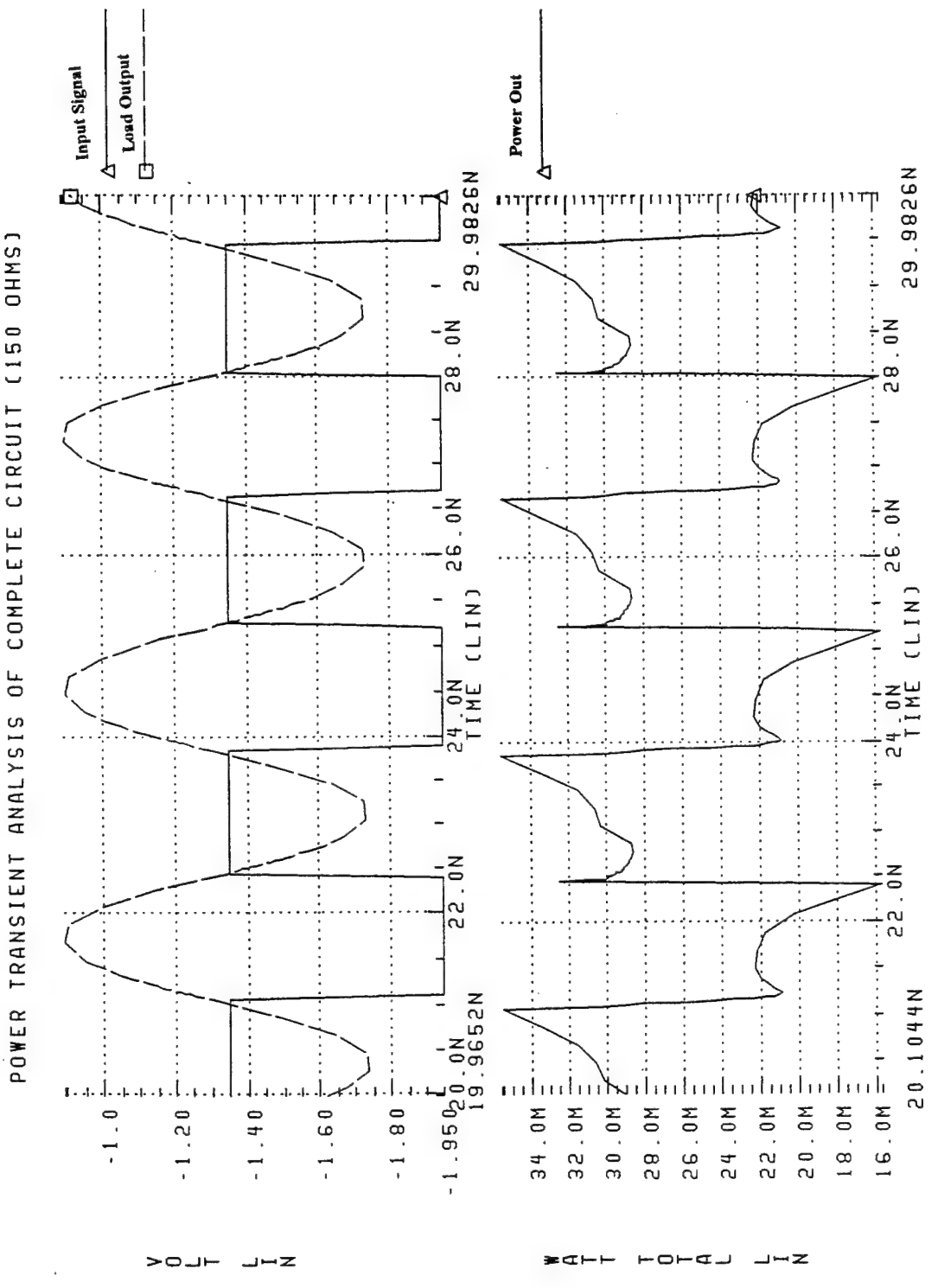

Figure 4-21 Transient Analysis of Complete Circuit (150 Ohms)

V. GALLIUM ARSENIDE IC DESIGN USING MAGIC

A. DRIVER LAYOUT FOR 50- , 100- , AND 150-OHM INTERCONNECT

The final consideration was to lay out the driver circuits using MAGIC and the Vitesse Semiconductor E/D MESFET design rules to see how much of a difference in layout area there is between the different driver circuits. The only transistor that is changed in each design is the source follower EFET. In the 50-ohm design, the size is 0.8 by 500 microns. This is much greater than in the 100-ohm design which uses only a 0.8 by 200 micron EFET. The 150-ohm circuit uses an EFET that is the smallest, only 0.8 by 120 microns. Since the size of this EFET affects the entire circuit, the circuit needed to be laid out to show just how much area each circuit covered. Figures 5-1 through 5-3 show the design and layout of the three different driver designs. In all three layouts, the transistor furthest to the right is the source follower EFET. The Figures show how the EFET changes from 50 Ohms, where the EFET is the largest transistor in the circuit, to 150 Ohms, where the EFET is comparable to the sizes of the other transistors.

The 50-ohm driver was the largest and the most difficult to design. Using interlaced EFETs connected together, the layout area was drastically reduced to a compact size (Figure 5-1). When completely finished, the bounding-box size was found to be 164 lambda by 340 lambda wide. The MAGIC HGaAs-III technology file has a lambda of 0.4 microns, which makes the size 65.6 microns by 136 microns, or 8,921.6 microns^2.

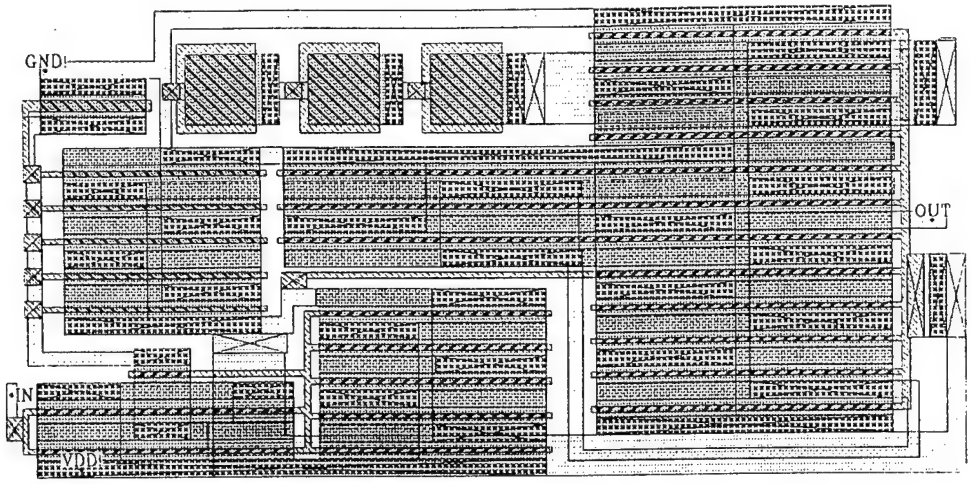

Figure 5-1 50-Ohm Driver Layout

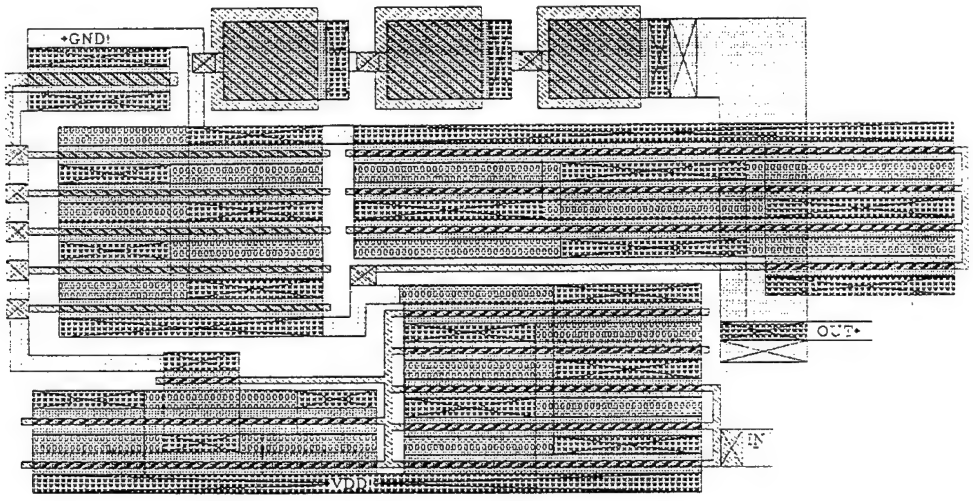

Figure 5-2 100-Ohm Driver Layout

The 40 percent decrease in size of the source follower EFET made a great difference in the size of the 100-ohm driver. The bounding box size for this layout was 153 by 256. This came out to a size of 65.6 by 102.4 microns, leaving an area of 6717.4

microns^2 (Figure 5-2).

In the 150-ohm driver design, the EFET size was almost as small as the other devices on the circuit and was much easier to lay out. The bounding box size of this layout was 152 by 201 lambda. This came out to 60.8 by 80.4 microns, an area of 4888.3 microns^2 (Figure 5-3).

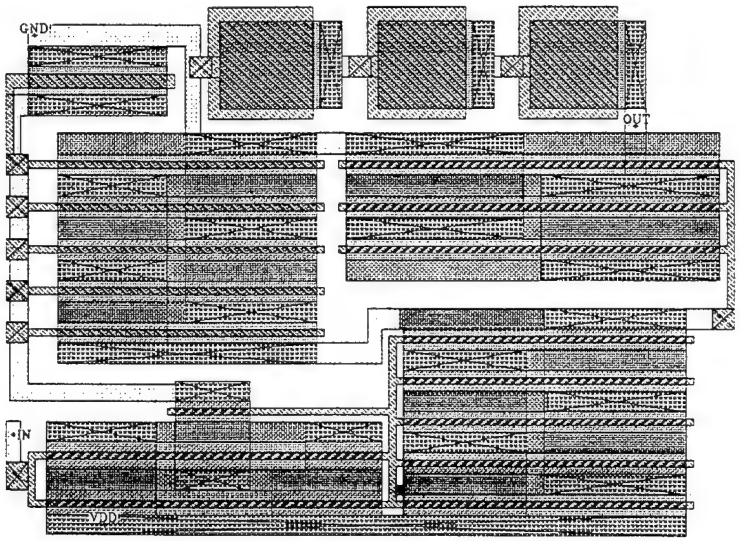

Figure 5-3 150-Ohm Driver Layout

The receiver circuit used is the same for all three driver circuits due to its high input impedance. The layout of the receiver was created to contrast the size of the receiver with the drivers. The bounding box area of the receiver was 72 by 34 lambda. This is 28.8 microns by 13.6 microns. This left an area of 391.7 microns^2 (Figure 5-4).

Figure 5-5 is a table comparing all drivers to each other. The difference in area

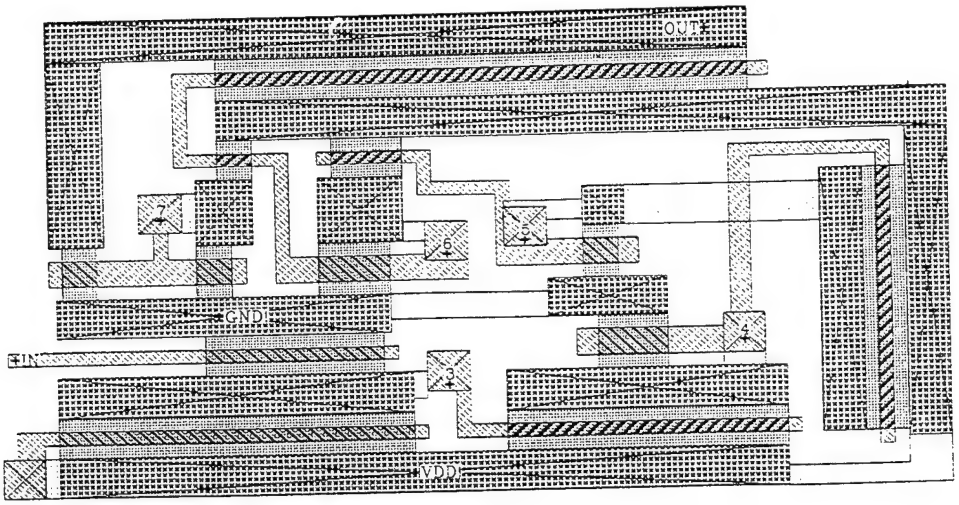

Figure 5-4 Receiver Layout

is shown to be significant. At 100 ohms, there is a 25-percent decrease in size. At 150-ohms, the decrease in size in 45 percent. This data shows just how much a change in interconnect impedance can affect a small chip.

	Dimensions	Area	Percentage of Area With Respect to 50 Ohm Driver
50 Ohm Driver	65.6 x 136 microns	8,921.6 microns^2	----------
100 Ohm Driver	65.6 x 102.4 microns	6,717.4 microns^2	75.3 %
150 Ohm Driver	60.8 x 80.4 microns	4,888 microns^2	54.8 %
Receiver	28.8 x 13.6 microns	391.7 microns^2	4.4 %

Figure 5-5 Area Comparison of Driver and Receiver Circuits

VI. CONCLUSIONS

A. POWER CONSUMPTION

The first goal of this project was to prove that there would be a significant decrease in power consumption for higher impedance interconnect compared to 50-ohm interconnect, the industry standard. After making some PCB calculations, it was found that the impedance could reasonably go no higher than 150 ohms because of manufacturing limitations. Using this information, three driver circuits were designed, simulated, and layed out. The assumption proved to be correct in practice. There was a 23 percent decrease in average power from the 50-ohm to the 100-ohm design. For the 150-ohm design, there was a 45 percent decrease in power. These results show a significant improvement in power reduction as the impedance is increased.

B. SPEED

At first, there was an assumption that since there was going to be a decrease in the size of the drivers as the impedance was increased, that there would also be a speedup in the circuit due to the decrease in gate capacitance. This did not prove to be the case. The 50-Ohm model reached a maximum frequency of 455 MHZ. The 100-Ohm and 150-Ohm, respectively, reached a maximum frequencies of 435 and 357 MHZ. The transition from 50 to 100 ohms netted a speed loss of 4.4 percent. The transition from 50 to 150 ohms netted a loss of 21.6 percent. The speed loss gets more significant

as the impedance is increased, and can become crucial in extremely high speed circuits.

C. LAYOUT AREA

The decrease in size was very significant between the 50-, 100- and 150-ohm circuits. There was a 25 percent difference from just 50 to 100 ohms and a 45 percent difference from 50 to 150 ohms. The size difference is large but is only limited to the driver circuit.

D. RECOMMENDATIONS

The major effect that the increase in impedance has on power consumption definitely validates further investigation into this area of study. Due to time constraints, fabrication of the chip and PCB were not available as an option. One important recommendation that should be noted is that the PCB itself turned out to be the limiting factor in the speed of the circuit. Further investigations into different PCB fabrication techniques and/or materials which could decrease the capacitance of the PCB could drastically affect the speed of the circuit when working with different impedances. For the purpose of this thesis, data from a local glass/epoxy PCB manufacturer were used. Polyamide or TEFLON PCB technology may help to decrease parasitic capacitance and increase speed.

Fabrication and testing of a PCB and GaAs test chip would enhance and further prove the results found, and could show other benefits as well.

The HSPICE program was invaluable to this thesis and really enhanced the results found with its graphic capabilities. The problem is that the program is set up on only

were times when these computers were used for normal computing, which meant that the program had to be accessed by rlogin, with only half of the processor available. The recommendation is that since this program is used by a small fraction of students, that the program be placed on a computer that is not available to the general student body, but to a controlled set of students requiring the program.

APPENDIX A: MATLAB CODE FOR IMPEDANCE CALCULATIONS

Micro.M

```
% Micro.M    Matlab M-File For Calculating Impedance Curves
% Hugh J. Huck III

APPXS.WPDAPPXS.WPDh1=input('input the smallest thickness of the dielectric ');
h2=input('input the largest thickness of the dielectric ');
hmid=(h2-h1)/100;
t=.0014;
w1=input('input the smallest width of the strip ');
w2=input('input the largest width of the strip ');
wmid=(w2-w1/100);
w=(w2-w1)/2;
h=(h1:hmid:h2);
diel=4.6;
figure(1)
z=31.64476.*(log((4.*h)./(0.67.*((0.8.*w1)+t))));
z1=31.64476.*(log((4.*h)./(0.67.*((0.8.*w)+t))));
z2=31.64476.*(log((4.*h)./(0.67.*((0.8.*w2)+t))));
plot(h,z,'r',h,z1,'g',h,z2,'y');
grid;
xlabel('dielectric thickness');
ylabel('Impedance');
gtext('Strip width of .005 inches');
gtext('Strip width of .0725 inches');
gtext('Strip width of .150 inches');
title('Microstrip Impedance Curves (t=.0014 inches)');
b1=2*(.0025)+t;
b2=.150;
b=(b1:(b2-b1)/100:b2);
figure(2)
g=27.9751.*log((4.*b)/(0.67.*pi.*(0.8.*w1)+t));
g1=27.9751.*log((4.*b)/(0.67.*pi.*(0.8.*w)+t));
g2=27.9751.*log((4.*b)/(0.67.*pi.*(0.8.*w2)+t));
plot(b,g,'r',b,g1,'g',b,g2,'y');
xlabel('Total dielectric thickness');
ylabel('Impedance');
grid;
title('Stripline Impedance Curves (t=.0014 inches)');
```

```
gtext('Strip width of .005 inches');
gtext('Strip width of .0725 inches');
gtext('Strip width of .150 inches');
```

APPENDIX B: HSPICE PCB CODE

This section contains the code that was used in Chapter II to calculate the DC plots and transmission line plots for the Printed Circuit Board.

FIGURE B-1 DC ANALYSIS OF PCB TRANSMISSION LINE

```
Thesis Transient Analysis Of Printed Circuit Board.
* Hugh J Huck III
* April 1 1996

* include Vitesse HGaAs3 models and parameters for hspice.
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
* Make the circuit sampling the highest accuracy
.OPTION POST RELVAR = 0.05
.OPTION ACCURATE
* Signal Source

.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=7.15n

* input signal
V1 1 0

* main circuit

Rdr    1 2 50
CBP1   2 0 620fF
LBW1   2 3 7.104nH
CPack1 3 0 154.2fF
U1     3 0 4 0 micro1 L=.0127
CBoard1 4 0 206.8fF
U2     4 0 5 0 micro2 L=0.3048
Rload  5 0 50
CBoard2 5 0 206.8fF
U3     5 0 6 0 micro1 L=.0127
CPack2 6 0 154.2fF
LBW2   6 7 7.104nH
CBP2   7 0 620fF

.dc V1 -3.6 -1.6 0.01
.END
```

Figure B-2 TRANSIENT ANALYSIS OF PCB TRANSMISSION LINE AT 50 OHMS

```
Thesis Transient Analysis of Printed Circuit Board.
*  Hugh J Huck III
*  April 11 1996

* include Vitesse HGaAs3 models and parameters for hspice.
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
* Make the circuit sampling the highest accuracy
.OPTION POST RELVAR = 0.05
.OPTION ACCURATE

* Signal Source
.tran 1p 8N
*transmission line models

* package
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=10.54n DELEN=1.0
VREL=0.316
* PCB
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=7.15n  DELEN=1.0
VREL=0.466

* input signal
V1 1 0  PULSE (-1.6 -0.9 0.0 125ps 125ps 875ps 2000ps)


* main circuit
* Voltage Driver Resistance
Rdr     1 2 50
* Bond Pad Capacitance
CBP1    2 0 620fF
* Bond Wire Inductance
LBW1    2 3 7.104nH
* Package Capacitance
CPack1  3 0 154.2fF
```

```
*transmission line of the package
U1      3 0 4 0 micro1 L=0.0127
* Capacitance of the Board
CBoard1 4 0 206.8fF
* Transmission line of the PCB
U2      4 0 5 0 micro2 L=0.3048
* Load Resistance
Rload   5 0 50
*Capacitance of the board
CBoard2 5 0 206.8fF
* Transmission line of the package
U3      5 0 6 0 micro1 L=0.0127
* Capacitance of the package
CPack2  6 0 154.2fF
* Inductance of the bond wire
LBW2    6 7 7.104nH
* Capacitance of the Bond pad
CBP2    7 0 620fF

.END
```

Figure B-3 TRANSIENT ANALYSIS OF PCB TRANSMISSION LINE AT 100 OHMS

```
Thesis Transient Analysis of Printed Circuit Board (100 Ohms).
*  Hugh J Huck III
*  April 1 1996

* include Vitesse HGaAs3 models and parameters for hspice.
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
* Make the circuit sampling the highest accuracy
.OPTION POST RELVAR = 0.05
.OPTION ACCURATE

* Signal Source
.tran 1p 8N

.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=100 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=100 DELAY=7.15n

V1 1 0  PULSE (-3.6 -1.6 0.0 250ps 250ps 1000ps 2500ps)
* main circuit

Rdr    1 2 100
CBP1   2 0 620fF
LBW1   2 3 7.104nH
CPack1 3 0 154.2fF
U1     3 0 4 0 micro1 L=.0127
CBoard1 4 0 206.8fF
U2     4 0 5 0 micro2 L=0.3048
Rload  5 0 100
CBoard2 5 0 206.8fF
U3     5 0 6 0 micro1 L=.0127
CPack2 6 0 154.2fF
LBW2   6 7 7.104nH
CBP2   7 0 620fF

.END
```

Figure B-4 TRANSIENT ANALYSIS OF PCB TRANSMISSION LINE AT 150 OHMS

```
Thesis Transient Analysis of Printed Circuit Board (150 Ohms).
*  Hugh J Huck III
*  April 1 1996

* include Vitesse HGaAs3 models and parameters for hspice.
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
* Make the circuit sampling the highest accuracy
.OPTION POST RELVAR = 0.05
.OPTION ACCURATE
* Signal Source
.tran 1p 8N

.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=150 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=150 DELAY=7.15n

V1 1 0  PULSE (-3.6 -1.6 0.0 50ps 50ps 1000ps 2000ps)

* main circuit

Rdr    1 2 150
CBP1   2 0 620fF
LBW1   2 3 7.104nH
CPack1  3 0 154.2fF
U1     3 0 4 0 micro1 L=.0127
CBoard1 4 0 206.8fF
U2     4 0 5 0 micro2 L=0.3048
Rload   5 0 150
CBoard2 5 0 206.8fF
U3     5 0 6 0 micro1 L=.0127
CPack2  6 0 154.2fF
LBW2   6 7 7.104nH
CBP2   7 0 620fF

.END
```

APPENDIX C: DRIVER DC/ TRANSIENT ANALYSIS CODE

This section contains the code in testing and evaluating the driver. Both DC and transient analysis are included. Interactions with the PCB transmission line model are also included.

Figure C-1 DC ANALYSIS OF DRIVER DESIGN AT 50 OHMS

```
Source Follower Driver Design (50 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect

* power supply
vds 1 0 -2.0

* input signal
vin 2 0

*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=500.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
r1 7 1 50

* analysis parameters
.options scale=1E-06 post
.dc vin  -1.95 -1.35 0.01
.end
```

Figure C-2 DC ANALYSIS OF DRIVER DESIGN AT 100 OHMS

```
 Source Follower Driver Design (100 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect

* power supply
vds 1 0 -2.0

* input signal
vin 2 0

*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=200.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
r1 7 1 100

* analysis parameters
.options scale=1E-06 post
.dc vin   -1.95 -1.35 0.01
.end
```

Figure C-3 DC ANALYSIS OF DRIVER DESIGN AT 150 OHMS

```
Source Follower Driver Design (150 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect

* power supply
vds 1 0 -2.0

* input signal
vin 2 0

*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=120.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
r1 7 1 150

* analysis parameters
.options scale=1E-06 post
.dc vin  -1.95 -1.35 0.01
.end
```

Figure C-4 DC ANALYSIS OF DRIVER CONNECTED TO TRANSMISSION LINE (50 OHMS)

```
Source Follower Driver Design Connected With Transmission Line Model
* Hugh J Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=7.15n
.plot DC P(j9) P(LBW2) P(vin) P(CBP2) POWER
* power supply
vds 1 0 -2.0

* input signal
vin 2 0

*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=500.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
U1     11 0 12 0 micro1 L=.0127
CBoard1 12 0 206.8fF
U2     12 0 13 0 micro2 L=0.3048
RLoad  13 1 50
```

```
CBoard2 13 0 206.8fF
U3      13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF


* analysis parameters
.options scale=1E-06 post
.dc vin   -1.95 -1.35 0.01
.end
```

Figure C-5 DC ANALYSIS OF DRIVER CONNECTED TO TRANSMISSION LINE (100 OHMS)

```
Source Follower Driver Design Connected With Transmission Line Model
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=100 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=100 DELAY=7.15n
.plot DC P(j9) P(LBW2) P(vin) P(CBP2) POWER

* power supply
vds 1 0 -2.0

* input signal
vin 2 0

*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=200.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
U1     11 0 12 0 micro1 L=.0127
CBoard1 12 0 206.8fF
U2     12 0 13 0 micro2 L=0.3048
```

```
RLoad  13 1 100
CBoard2 13 0 206.8fF
U3      13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF


* analysis parameters
.options scale=1E-06 post
.dc vin   -1.95 -1.35 0.01
.end
```

Figure C-6 DC ANALYSIS OF DRIVER CONNECTED TO TRANSMISSION LINE (150 OHMS)

```
Source Follower Driver Design Connected with Transmission Line Model (150 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=150 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=150 DELAY=7.15n
.plot DC P(j9) P(LBW2) P(vin) P(CBP2) POWER

* power supply
vds 1 0 -2.0

* input signal
vin 2 0

*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=120.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
U1     11 0 12 0 micro1 L=.0127
CBoard1 12 0 206.8fF
U2     12 0 13 0 micro2 L=0.3048
```

```
RLoad  13 1 150
CBoard2 13 0 206.8fF
U3      13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF



* analysis parameters
.options scale=1E-06 post
.dc vin   -1.95 -1.35 0.01
.end
```

Figure C-7 TRANSIENT ANALYSIS OF PCB INTERCONNECT AND DRIVER AT 50 OHMS

```
Source Follower Transient Design Connected With Transmission Line (50 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.options scale=1E-06 post
.tran 100p 12.5n

.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=7.15n
.plot tran P(j9) P(LBW2) P(vin) P(CBP2) POWER
* power supply
vds 1 0 -2.0

* input signal
vin 2 0  PULSE (-1.95 -1.35 0.0 50ps 50ps 1200ps 2400ps)


*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=500.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0

CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
U1     11 0 12 0 micro1 L=.0127
CBoard1 12 0 206.8fF
```

```
U2      12 0 13 0 micro2 L=0.3048
RLoad  13 1 50
CBoard2 13 0 206.8fF
U3      13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF


* analysis parameters


.end
```

Figure C-8 TRANSIENT ANALYSIS OF PCB INTERCONNECT AND DRIVER AT 100 OHMS

```
Source Follower Transient Design Connected With Transmission Line (100 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.options scale=1E-06 post
.tran 100p 25n

.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=100 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=100 DELAY=7.15n
.plot tran P(j9) P(LBW2) P(vin) P(CBP2) POWER
* power supply
vds 1 0 -2.0

* input signal
vin 2 0  PULSE (-1.95 -1.35 0.0 200ps 200ps 1200ps 2400ps)


*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=200.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0

CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
U1     11 0 12 0 micro1 L=.0127
CBoard1 12 0 206.8fF
```

```
U2      12 0 13 0 micro2 L=0.3048
RLoad  13 1 100
CBoard2 13 0 206.8fF
U3      13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF


* analysis parameters


.end
```

Figure C-9 TRANSIENT ANALYSIS OF PCB INTERCONNECT AND DRIVER AT 150 OHMS

```
Source Follower Transient Design Connected With Transmission Line (150 Ohms)
* Hugh J. Huck III
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.options scale=1E-06 post
.tran 100p 25n
*.tran 1n 75n
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=150 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=150 DELAY=7.15n
.plot tran P(j9) P(LBW2) P(vin) P(CBP2) POWER

* power supply
vds 1 0 -2.0

* input signal
vin 2 0  PULSE (-1.95 -1.35 0.0 250ps 250ps 1200ps 2400ps)

*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=120.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*r1 7 1 150

CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
```

```
U1     11 0 12 0 micro1 L=.0127
CBoard1 12 0 206.8fF
U2     12 0 13 0 micro2 L=0.3048
RLoad  13 1 150
CBoard2 13 0 206.8fF
U3     13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF


* analysis parameters


.end
```

APPENDIX D: RECEIVER DC / TRANSIENT ANALYSIS CODE

This section contains the code in testing and evaluating the receiver circuit. Both DC and transient analysis are included. Code for the entire circuit, both DC and transient analysis is included in this appendix.

Figure D-1 DC ANALYSIS OF RECEIVER DESIGN

```
DC Analysis of Receiver Design (50 Ohms)
* Hugh J. Huck III
  .protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=7.15n
.plot DC POWER

* power supply
vds 1 0 -2.0

* input signal
vin 2 0

*main circuit
j1 0 2 3 1 dp1.1 l=0.8 w=10.0
j2 3 1 1 1 dp1.1 l=0.8 w=20.0

j3 0 4 4 1 dp1.1 l=1.6 w=4.0
j4 4 3 1 1 enh.1 l=0.8 w=16.0

j5 0 5 5 1 dp1.1 l=1.6 w=2.0
j6 5 4 1 1 enh.1 l=0.8 w=16.0

j7 0 6 6 1 dp1.1 l=1.6 w=4.0
j8 6 5 1 1 enh.1 l=0.8 w=4.0

j9 0 7 7 1 dp1.1 l=1.6 w=2.0
j10 7 6 1 1 enh.1 l=0.8 w=2.0

j11 0 7 8 1 dp1.1 l=1.6 w=2.0
j12 8 6 1 1 enh.1 l=0.8 w=30.0
 * analysis parameters
.options scale=1E-06 post
.dc vin  -1.8 -0.8 0.01
.end
```

Figure D-2 TRANSIENT ANALYSIS OF RECEIVER DESIGN

```
 Receiver Design
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=7.15n
.plot DC POWER
.options scale=1E-06 post
.tran 100p 4n

* power supply
vds 1 0 -2.0
* input signal
vin 2 0  PULSE (-1.8 -0.8 0.0 50ps 50ps 500ps 1ns)
*main circuit

j1 0 2 3 1 dp1.1 l=0.8 w=10.0
j2 3 1 1 1 dp1.1 l=0.8 w=20.0

j3 0 4 4 1 dp1.1 l=1.6 w=4.0
j4 4 3 1 1 enh.1 l=0.8 w=16.0

j5 0 5 5 1 dp1.1 l=1.6 w=2.0
j6 5 4 1 1 enh.1 l=0.8 w=16.0

j7 0 6 6 1 dp1.1 l=1.6 w=4.0
j8 6 5 1 1 enh.1 l=0.8 w=4.0

j9 0 7 7 1 dp1.1 l=1.6 w=2.0
j10 7 6 1 1 enh.1 l=0.8 w=2.0

j11 0 7 8 1 dp1.1 l=1.6 w=2.0
j12 8 6 1 1 enh.1 l=0.8 w=30.0

.end
```

Figure D-3 TRANSIENT ANALYSIS OF COMPLETE CIRCUIT AT 50 OHMS

```
Transient Analysis of Complete Circuit (50 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=50 DELAY=7.15n
.plot DC POWER
.options scale=1E-06 post
.tran 100p 40n

* power supply
vds 1 0 -2.0

* input signal
vin 2 0  PULSE (-1.95 -1.35 0.0 5ps 5ps 1.1ns 2.2ns)


*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=500.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
U1     11 0 12 0 micro1 L=.0127
```

```
CBoard1 12 0 206.8fF
U2      12 0 13 0 micro2 L=0.3048
RLoad  13 1 50
CBoard2 13 0 206.8fF
U3      13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF



*main circuit

j10 0 15 16 1 dp1.1 l=0.8 w=10.0
j12 16 1 1 1 dp1.1 l=0.8 w=20.0

j13 0 17 17 1 dp1.1 l=1.6 w=4.0
j14 17 16 1 1 enh.1 l=0.8 w=16.0

j15 0 18 18 1 dp1.1 l=1.6 w=2.0
j16 18 17 1 1 enh.1 l=0.8 w=16.0

j17 0 19 19 1 dp1.1 l=1.6 w=4.0
j18 19 18 1 1 enh.1 l=0.8 w=4.0

j19  0 20 20 1 dp1.1 l=1.6 w=2.0
j20 20 19 1 1 enh.1 l=0.8 w=2.0

j21 0 20 21 1 dp1.1 l=1.6 w=2.0
j22 21 19 1 1 enh.1 l=0.8 w=30.0


.end
```

Figure D-4 TRANSIENT ANALYSIS OF COMPLETE CIRCUIT AT 100 OHMS

```
Transient Analysis of Complete Circuit (100 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=100 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=100 DELAY=7.15n
.plot DC POWER
.options scale=1E-06 post
.tran 100p 40n

* power supply
vds 1 0 -2.0

* input signal
vin 2 0  PULSE (-1.95 -1.35 0.0 50ps 50ps 1.15ns 2.3ns)


*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=200.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
U1     11 0 12 0 micro1 L=.0127
```

```
CBoard1 12 0 206.8fF
U2      12 0 13 0 micro2 L=0.3048
RLoad  13 1 100
CBoard2 13 0 206.8fF
U3      13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF



*main circuit
j10 0 15 16 1 dp1.1 l=0.8 w=10.0
j12 16 1 1 1 dp1.1 l=0.8 w=20.0

j13 0 17 17 1 dp1.1 l=1.6 w=4.0
j14 17 16 1 1 enh.1 l=0.8 w=16.0

j15 0 18 18 1 dp1.1 l=1.6 w=2.0
j16 18 17 1 1 enh.1 l=0.8 w=16.0

j17 0 19 19 1 dp1.1 l=1.6 w=4.0
j18 19 18 1 1 enh.1 l=0.8 w=4.0

j19  0 20 20 1 dp1.1 l=1.6 w=2.0
j20 20 19 1 1 enh.1 l=0.8 w=2.0

j21 0 20 21 1 dp1.1 l=1.6 w=2.0
j22 21 19 1 1 enh.1 l=0.8 w=30.0

.end
```

Figure D-5 TRANSIENT ANALYSIS OF COMPLETE CIRCUIT AT 150 OHMS

```
Transient Analysis of Complete Circuit (150 Ohms)
* Hugh J. Huck III

.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect
.model micro1 U LEVEL=3 ELEV=3 PLEV=1 ZK=150 DELAY=10.54n
.model micro2 U LEVEL=3 ELEV=3 PLEV=1 ZK=150 DELAY=7.15n
.plot DC POWER
.options scale=1E-06 post
.tran 100p 40n

* power supply
vds 1 0 -2.0

* input signal
vin 2 0  PULSE (-1.95 -1.35 0.0 50ps 50ps 1.4ns 2.8ns)


*main circuit
j1 0 3 3 1 dp1.1 l=1.6 w=15.0
j2 3 2 1 1 enh.1 l=0.8 w=60.0
*Important one
j3 0 3 4 1 dp1.1 l=0.8 w=130.0
j4 4 2 1 1 enh.1 l=0.8 w=150.0

j6 6 0 6 1 dp1.1 l=10.0 w=10.0
j7 9 6 9 1 dp1.1 l=10.0 w=10.0
j8 0 4 7 1 enh.1 l=0.8 w=120.0
j9 7 9 7 1 dp1.1 l=10.0 w=10.0


*resistance
CBP1   7 0 620fF
LBW1   7 11 7.104nH
CPack1 11 0 154.2fF
U1     11 0 12 0 micro1 L=.0127
```

```
CBoard1 12 0 206.8fF
U2      12 0 13 0 micro2 L=0.3048
RLoad  13 1 150
CBoard2 13 0 206.8fF
U3      13 0 14 0 micro1 L=.0127
CPack2 14 0 154.2fF
LBW2   14 15 7.104nH
CBP2   15 0 620fF


*main circuit

j10 0 15 16 1 dp1.1 l=0.8 w=10.0
j12 16 1 1 1 dp1.1 l=0.8 w=20.0

j13 0 17 17 1 dp1.1 l=1.6 w=4.0
j14 17 16 1 1 enh.1 l=0.8 w=16.0

j15 0 18 18 1 dp1.1 l=1.6 w=2.0
j16 18 17 1 1 enh.1 l=0.8 w=16.0

j17 0 19 19 1 dp1.1 l=1.6 w=4.0
j18 19 18 1 1 enh.1 l=0.8 w=4.0

j19  0 20 20 1 dp1.1 l=1.6 w=2.0
j20 20 19 1 1 enh.1 l=0.8 w=2.0

j21 0 20 21 1 dp1.1 l=1.6 w=2.0
j22 21 19 1 1 enh.1 l=0.8 w=30.0

.end
```

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